EE 330
Lecture 42

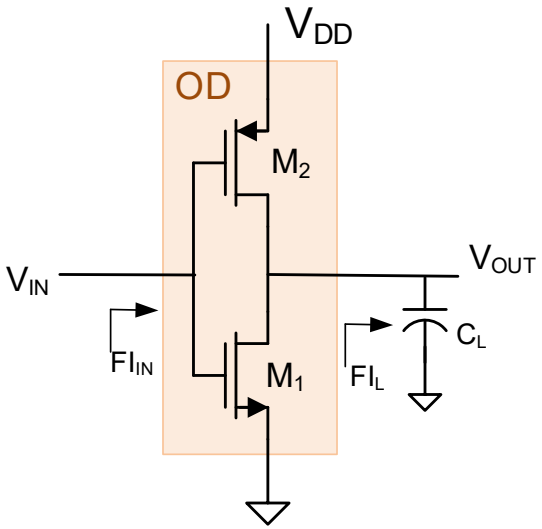
Digital Circuits

- Propagation Delay with Various Sizing
- Optimally driving large capacitive loads
- Logic Effort Method for Signal Propagation

Spring 2024 Exam Schedule

Exam 1 Friday Feb 16
Exam 2 Friday March 8
Exam 3 Friday April 19
Final Exam Tuesday May 7 7:30 AM - 9:30 AM

Overdrive Factors



Scaling widths of ALL devices by constant (W_{scaled}=WxOD) will change "drive" capability relative to that of the reference inverter but not change relative value of t_{HL} and t_{LH}

$$R_{PD}=\frac{L_1}{\mu_n C_{OX} W_1 (V_{DD}-V_{Tn})} \rightarrow R_{PDOD}=\frac{L_1}{\mu_n C_{OX} [OD \bullet W_1](V_{DD}-V_{Tn})}=\frac{R_{PD}}{OD}$$

$$R_{PU}=\frac{L_2}{\mu_p C_{OX} W_2 (V_{DD}+V_{Tp})} \rightarrow R_{PUOD}=\frac{L_2}{\mu_p C_{OX} [OD \bullet W_2](V_{DD}+V_{Tp})}=\frac{R_{PU}}{OD}$$

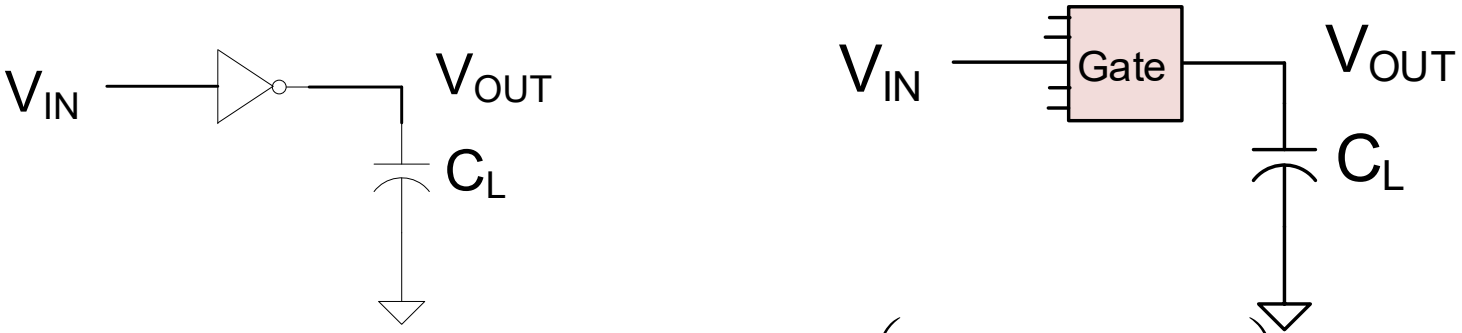
$$t_{PROP}=t_{REF} \bullet FI_L \bullet \frac{1}{OD}$$

Scaling widths of ALL devices by constant will change FI_{IN} to gate by OD

$$C_{IN}=C_{OX}(W_1L_1+W_2L_2) \rightarrow C_{INOD}=C_{OX}([OD \bullet W_1]L_1+[OD \bullet W_2]L_2)=OD \bullet C_{IN}$$

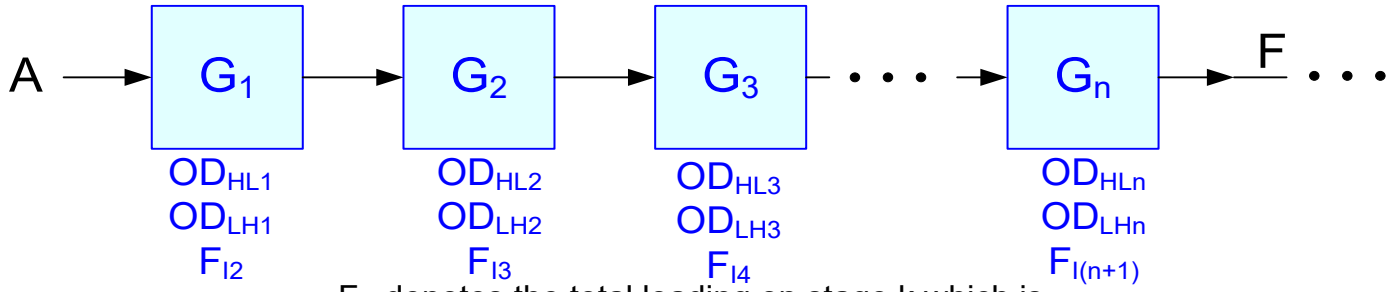
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric Overdrive



$$t_{PROP} = t_{HL} + t_{LH} = \frac{1}{2} t_{REF} F_{ILOAD} \left(\frac{1}{OD_{HL}} + \frac{1}{OD_{LH}} \right)$$

When propagating through n stages:



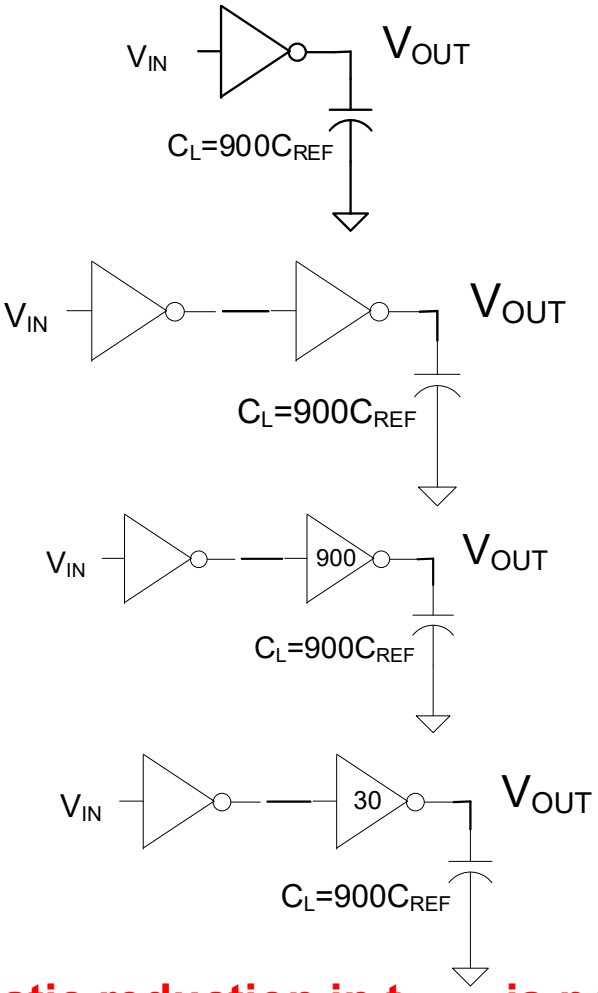
F_{Ik} denotes the total loading on stage k which is the sum of the F_I of all loading on stage k

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

Propagation Delay with Over-drive Capability

Example

Compare the propagation delays. Assume the OD is 900 in the third case and 30 in the fourth case. Don't worry about the extra inversion at this time.



$$t_{PROP} = 900t_{REF}$$

$$t_{PROP} = t_{REF} + 900t_{REF} = 901t_{REF}$$

$$t_{PROP} = 900t_{REF} + t_{REF} = 901t_{REF}$$

$$t_{PROP} = 30t_{REF} + 30t_{REF} = 60t_{REF}$$

- **Dramatic reduction in t_{PROP} is possible** (input is driving same in all 3 cases)
- **Will later determine what optimal number of stages and sizing is**

Propagation Delay in Multiple-Levels of Logic with Stage Loading

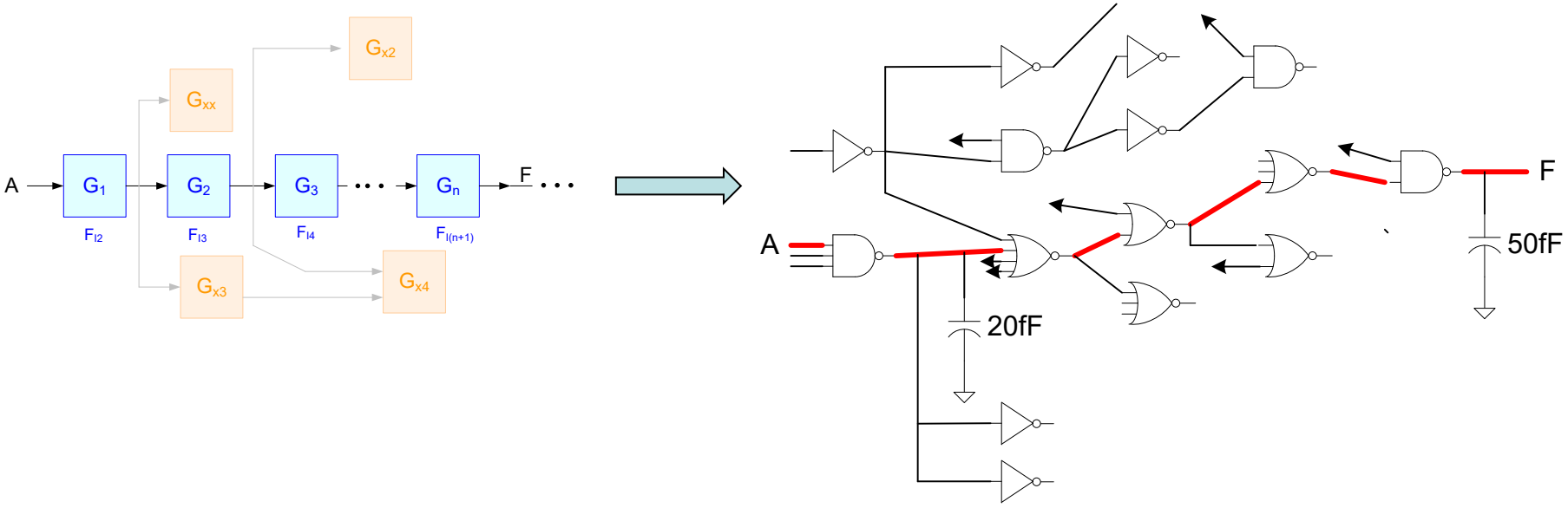
Will consider an example with the five cases

- **Equal rise/fall (no overdrive)**
- **Equal rise/fall with overdrive**
- **Minimum Sized**
- **Asymmetric Overdrive**
- **Combination of equal rise/fall, minimum size and overdrive**

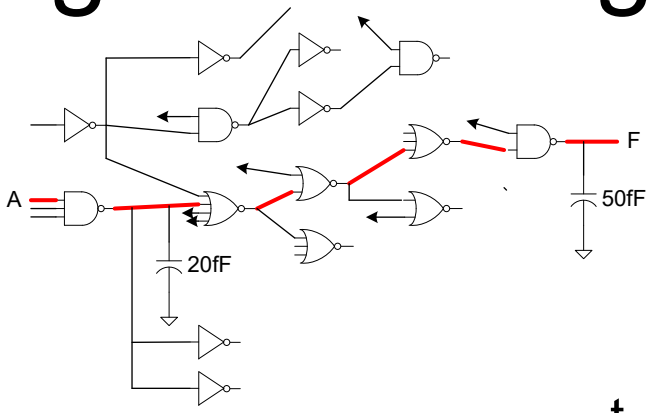
Will develop the analysis methods as needed

Propagation Delay in Multiple-Levels of Logic with Stage Loading and Overdrives

Will now consider A to F propagation for this circuit as an example with different overdrives



Propagation Delay in Multiple-Levels of Logic with Stage Loading



- **Equal rise/fall (no overdrive)**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

- **Equal rise/fall with overdrive**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Minimum Sized**

$$t_{PROP} = \ ?$$

- **Asymmetric Overdrive**

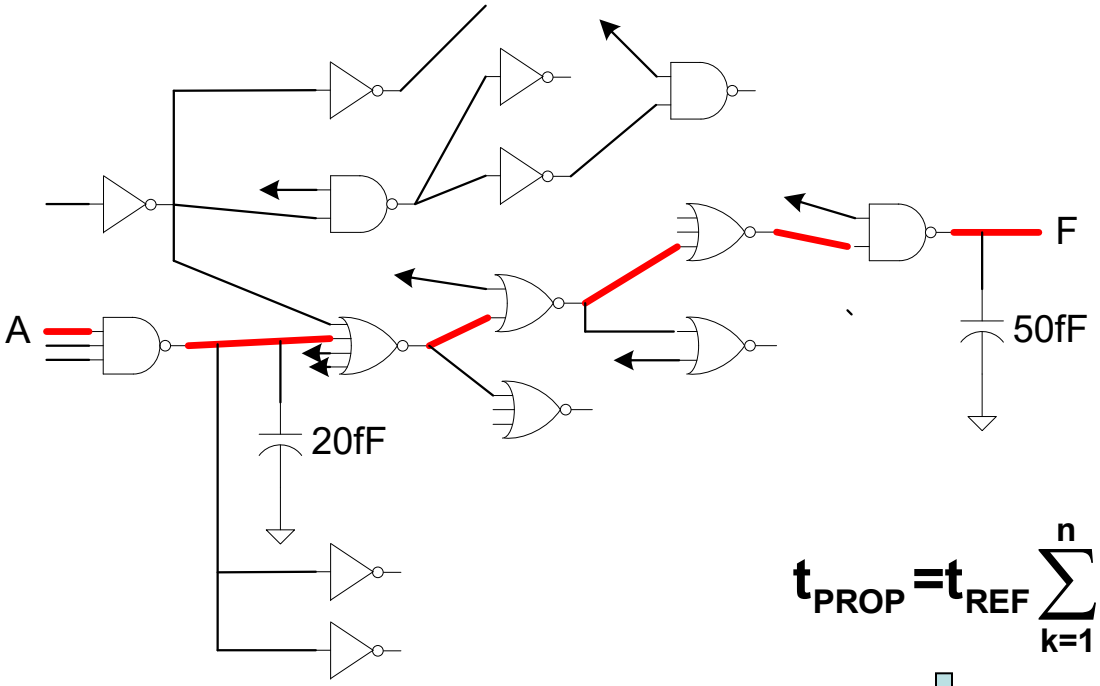
$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Combination of equal rise/fall, minimum size and overdrive**

$$t_{PROP} = \ ?$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, no overdrive



$$t_{PROP} = t_{REF} \sum_{k=1}^{n} F_{I_{k+1}}$$

$$\Downarrow$$

$$\frac{t_{PROP}}{t_{REF}} = \sum_{k=1}^{n} F_{I_{k+1}}$$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

Propagation Delay in Multiple-Levels of Logic with Stage Loading

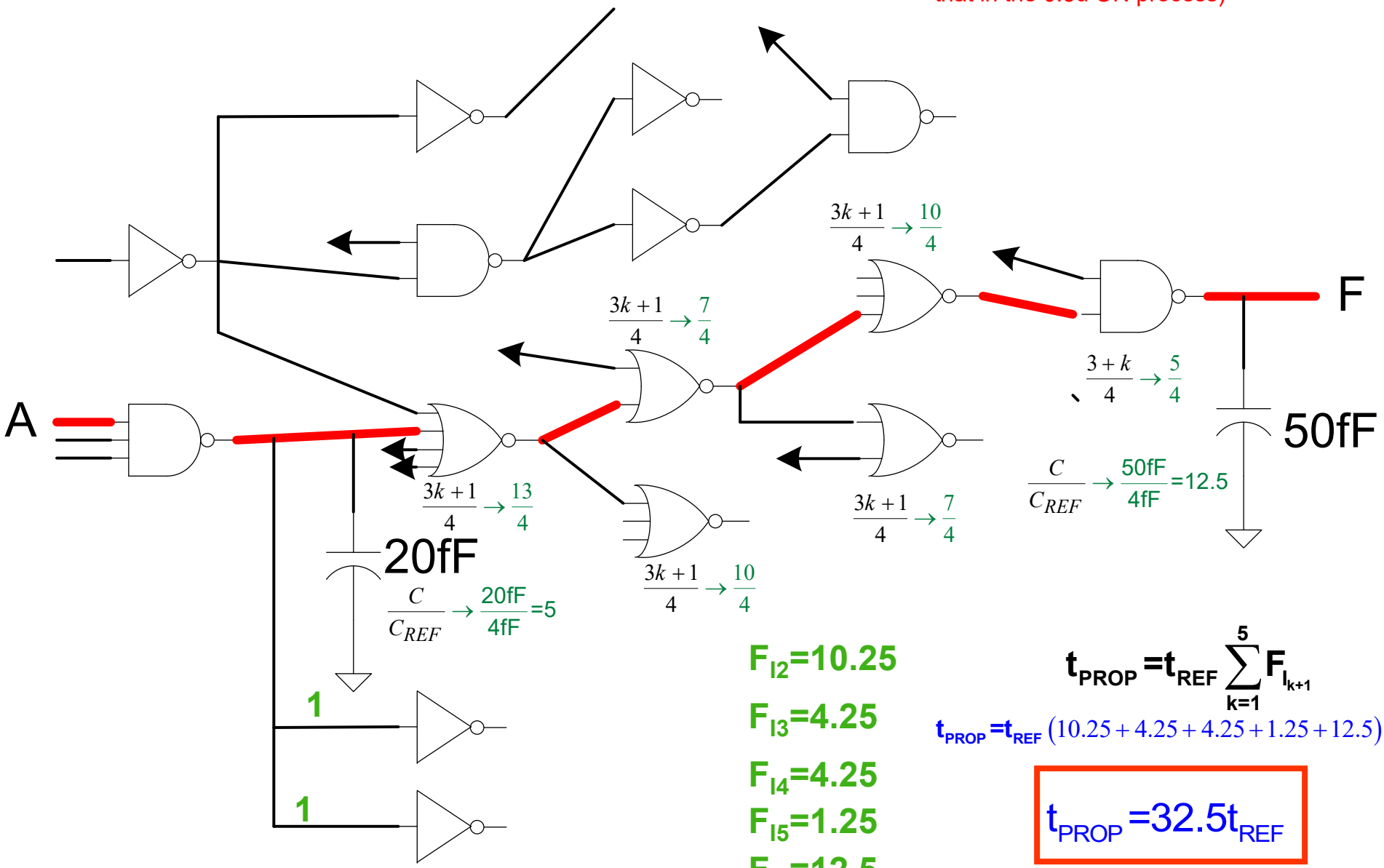
Equal rise-fall gates, no overdrive

	Equal Rise/Fall
C_{IN}/C_{REF}	
Inverter	1
NOR	$\frac{3k+1}{4}$
NAND	$\frac{3+k}{4}$
Overdrive	
Inverter	
HL	1
LH	1
NOR	
HL	1
LH	1
NAND	
HL	1
LH	1
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$

Equal rise-fall gates, no overdrive

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)



F_{I2}=10.25

F_{I3}=4.25

F_{I4}=4.25

F_{I5}=1.25

F_{I6}=12.5

$$t_{PROP} = t_{REF} \sum_{k=1}^{5} F_{I_{k+1}}$$

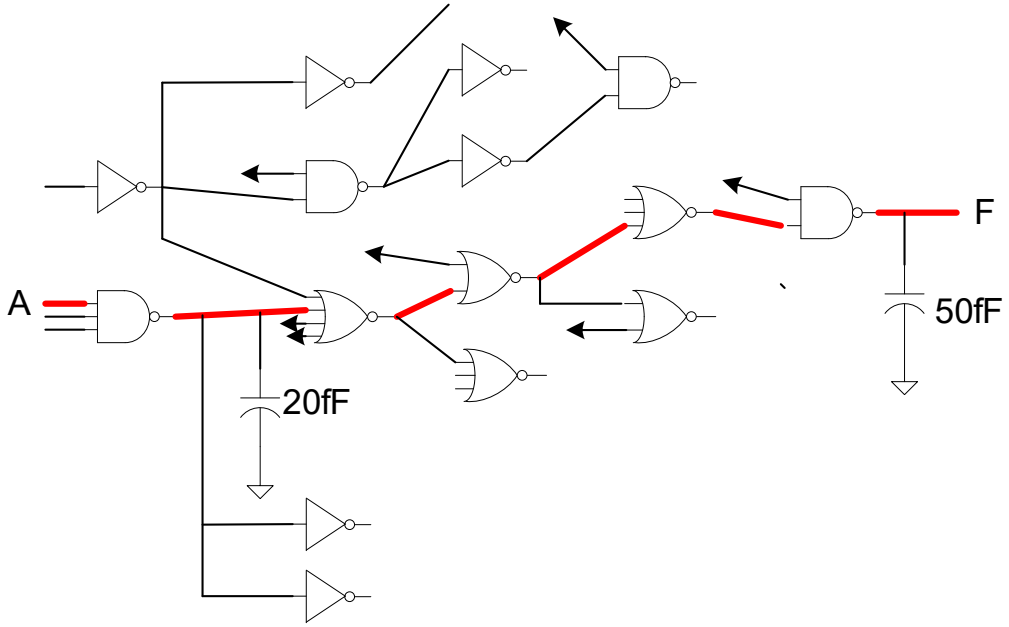
$$t_{PROP} = t_{REF} (10.25 + 4.25 + 4.25 + 1.25 + 12.5)$$

$$t_{PROP} = 32.5 t_{REF}$$

Equal rise-fall gates, no overdrive

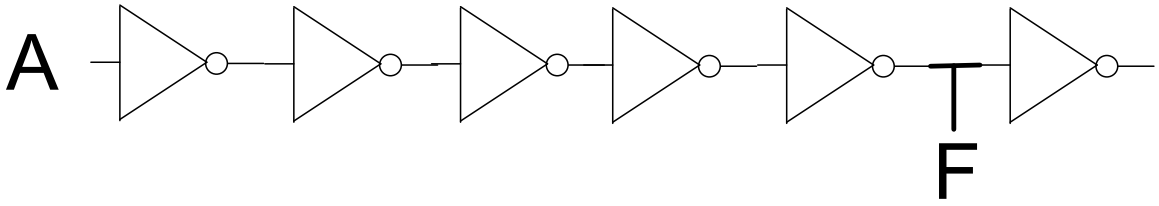
In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)



$t_{PROP}=32.5t_{REF}$

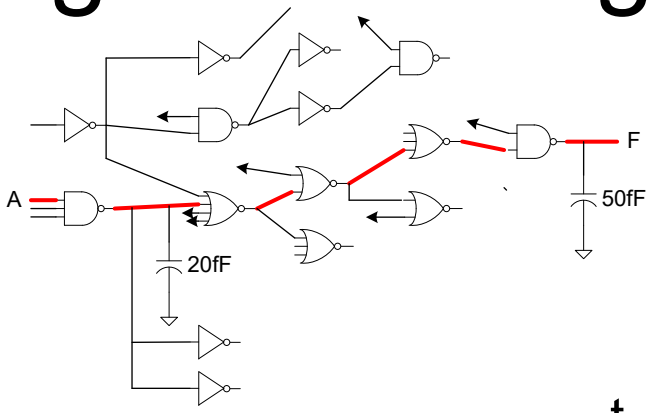
How does this propagation delay compare to that required for a propagation of a signal through 5-levels of logic with only reference inverters (load is a ref inverter instead of 50fF as well)?



$t_{PROP}=5t_{REF}$

Loading can have a dramatic effect on propagation delay

Propagation Delay in Multiple-Levels of Logic with Stage Loading



- **Equal rise/fall (no overdrive)**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

- **Equal rise/fall with overdrive**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Minimum Sized**

$$t_{PROP} = \ ?$$

- **Asymmetric Overdrive**

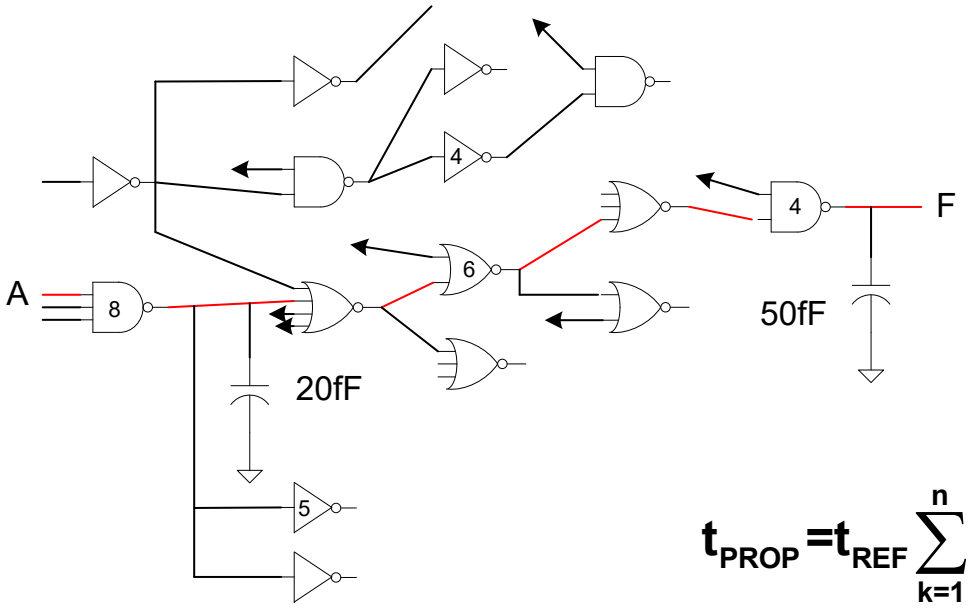
$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Combination of equal rise/fall, minimum size and overdrive**

$$t_{PROP} = \ ?$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overdrive



$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I_{k+1}}}{OD_k}$$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

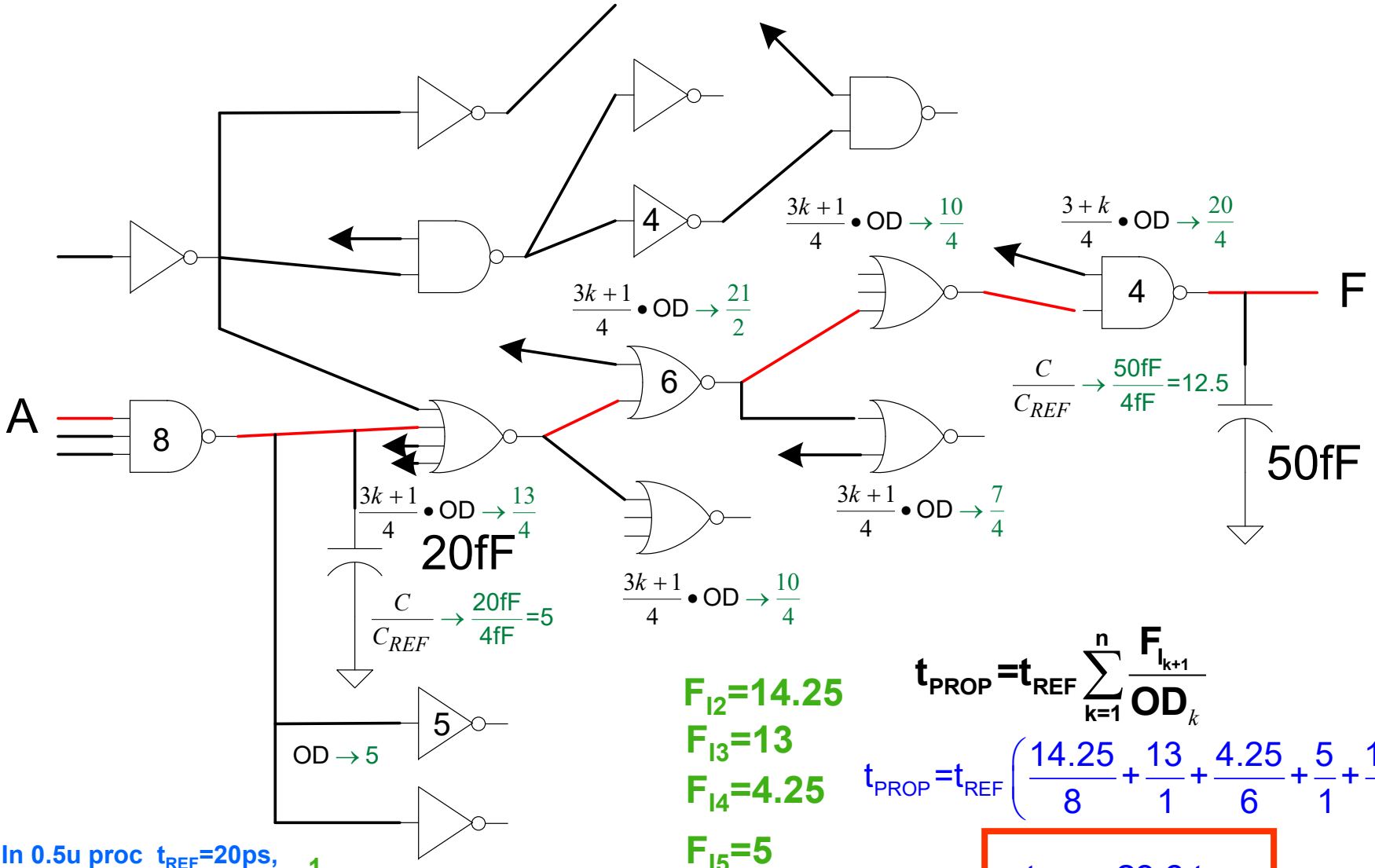
$$\frac{t_{PROP}}{t_{REF}} = \sum_{k=1}^{n} \frac{F_{I_{k+1}}}{OD_k}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Equal rise-fall gates, with overdrive

	Equal Rise/Fall	Equal Rise/Fall (with OD)
C_{IN}/C_{REF}		
Inverter	1	OD
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$
Overdrive		
Inverter		
HL	1	OD
LH	1	OD
NOR		
HL	1	OD
LH	1	OD
NAND		
HL	1	OD
LH	1	OD
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$

Equal rise-fall gates, with overdrive



$F_{I2}=14.25$

$F_{I3}=13$

$F_{I4}=4.25$

$F_{I5}=5$

$F_{I6}=12.5$

$$t_{PROP}=t_{REF}\sum_{k=1}^{n}\frac{F_{I_{k+1}}}{OD_k}$$

$$t_{PROP}=t_{REF}\left(\frac{14.25}{8}+\frac{13}{1}+\frac{4.25}{6}+\frac{5}{1}+\frac{12.5}{4}\right)$$

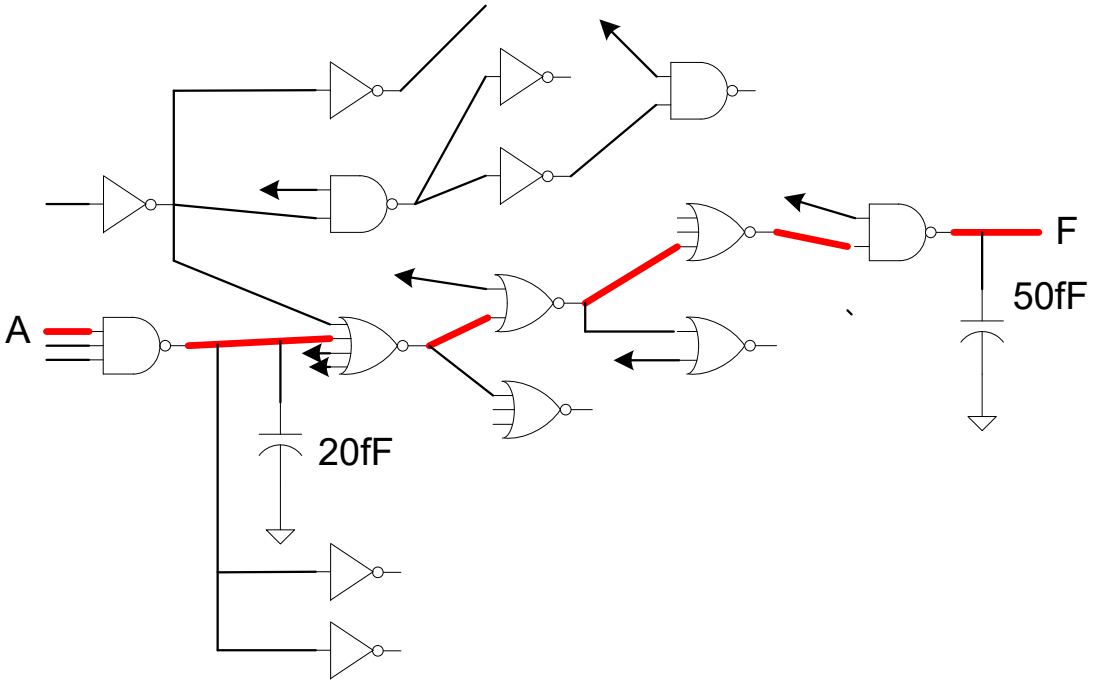
$$t_{PROP}=23.6\ t_{REF}$$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

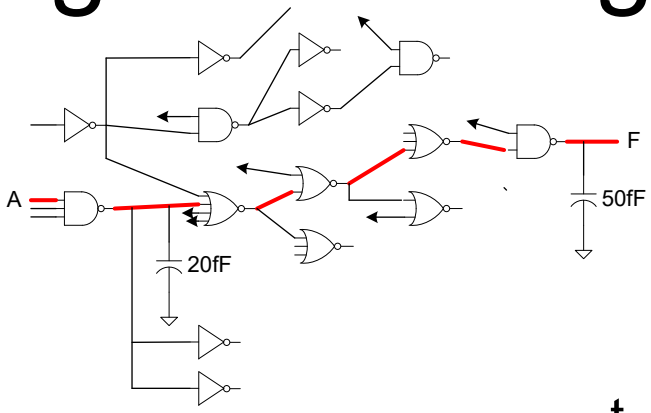


In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

$$t_{PROP} = t_{REF} \bullet ?$$

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)

Propagation Delay in Multiple-Levels of Logic with Stage Loading



- **Equal rise/fall (no overdrive)**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

- **Equal rise/fall with overdrive**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Minimum Sized**

$$t_{PROP} = \ ?$$

- **Asymmetric Overdrive**

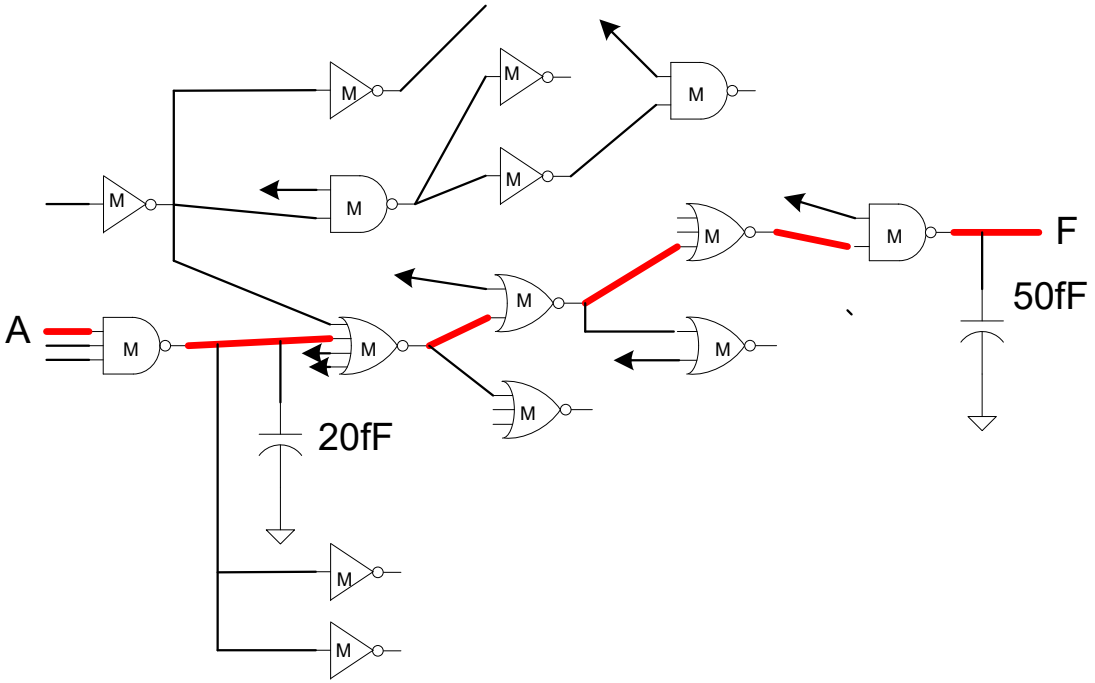
$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Combination of equal rise/fall, minimum size and overdrive**

$$t_{PROP} = \ ?$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

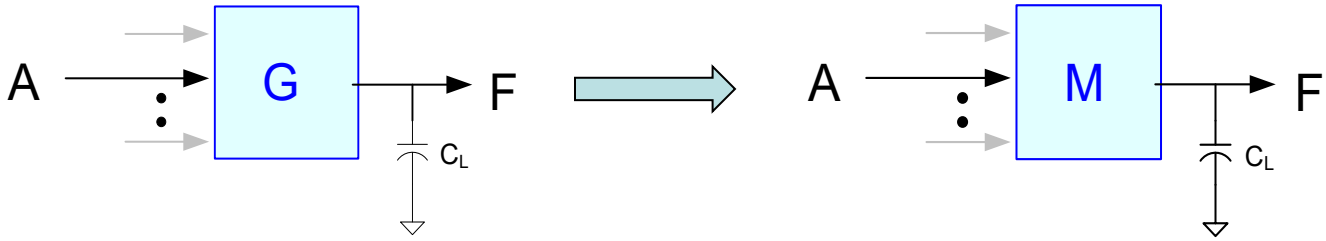
Minimum-sized gates



$t_{PROP} = t_{REF} \bullet ?$

Observe that a minimum-sized gate is simply a gate with asymmetric overdrive

Propagation Delay with Minimum-Sized Gates



Recall propagation delay for asymmetric overdrive:

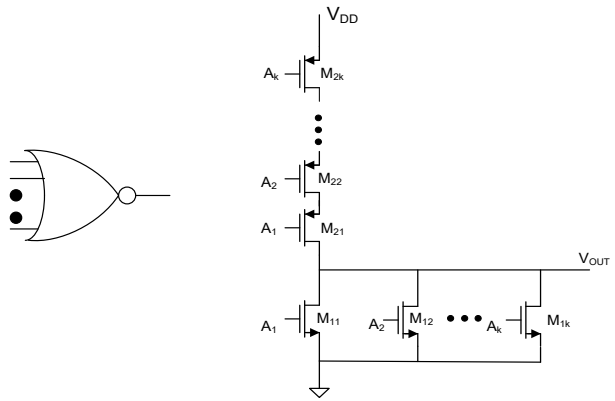
$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

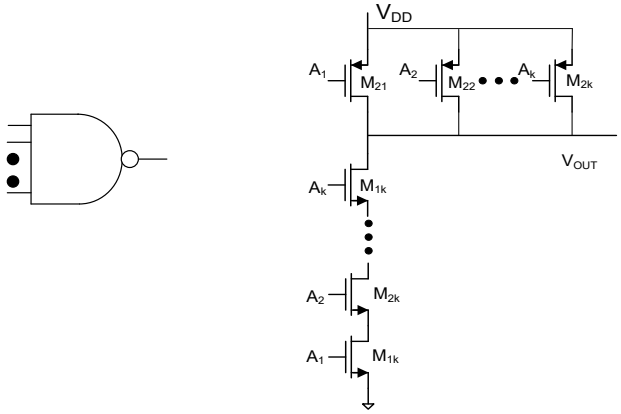
Thus for minimum-sized devices:

$$\frac{t_{PROP}}{t_{REF}} = \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Still need OD_{HL} and OD_{LH} for minimum-sized gates**
- **Still need FI for minimum-sized gates**

Propagation Delay with minimum-sized gates





$OD_{HL}=?$

$OD_{HL}=1$

$OD_{LH}=?$

$OD_{LH}=\frac{1}{3k}$

$OD_{HL}=?$

$OD_{HL}=1/k$

$OD_{LH}=?$

$OD_{LH}=\frac{1}{3}$

$$FI=2C_{OX}W_{MIN}L_{MIN}$$

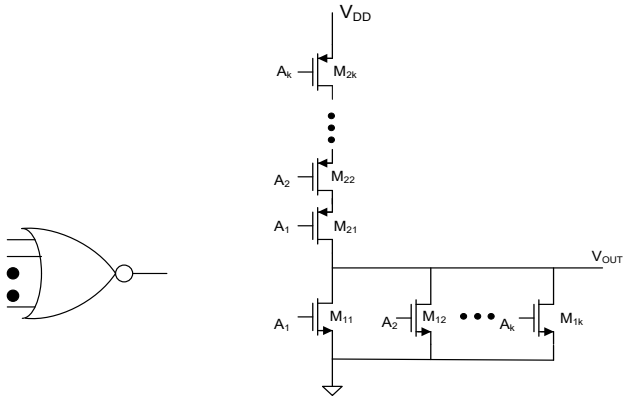
$$C_{REF}=4C_{OX}W_{MIN}L_{MIN}$$

$$FI=\frac{C_{REF}}{2}$$

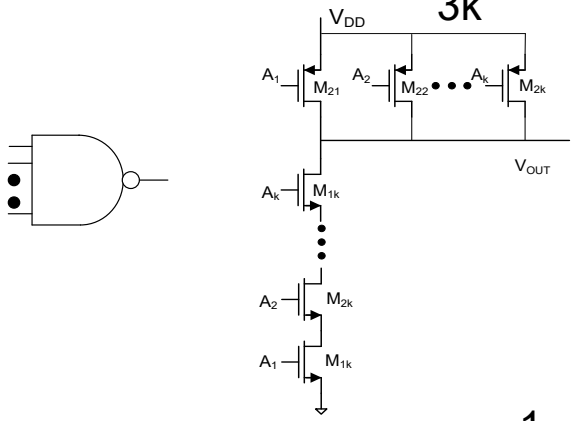
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized
C_{IN}/C_{REF}			
Inverter	1	OD	
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	
Overdrive			
Inverter			
HL	1	OD	
LH	1	OD	
NOR			
HL	1	OD	
LH	1	OD	
NAND			
HL	1	OD	
LH	1	OD	
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	



$OD_{HL}=1$ $\quad OD_{LH}=\frac{1}{3k}$



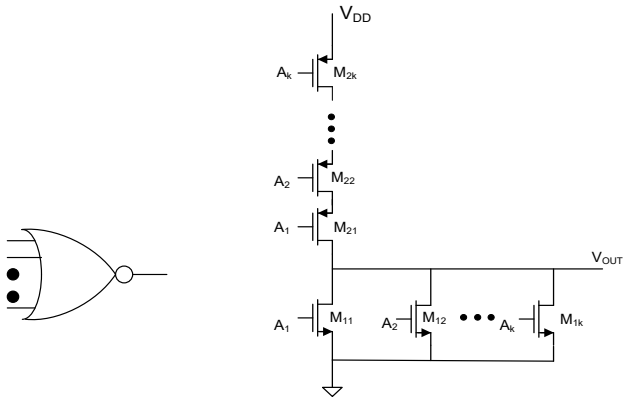
$OD_{HL}=1/k$ $\quad OD_{LH}=\frac{1}{3}$

$$FI=\frac{C_{REF}}{2}$$

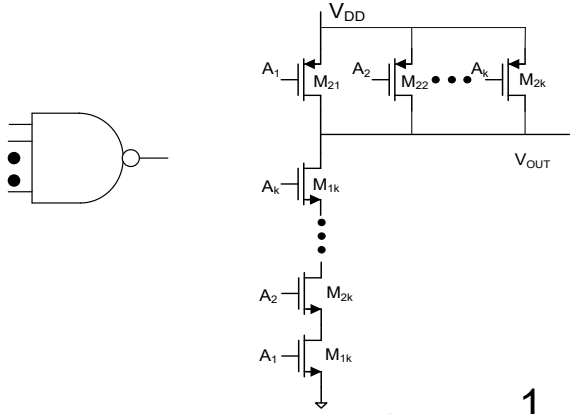
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized
C_{IN}/C_{REF}			
Inverter	1	OD	1/2
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4}\bullet OD$	1/2
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4}\bullet OD$	1/2
Overdrive			
Inverter			
HL	1	OD	1
LH	1	OD	1/3
NOR			
HL	1	OD	1
LH	1	OD	1/(3k)
NAND			
HL	1	OD	1/k
LH	1	OD	1/3
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$



$OD_{HL}=1$ $\quad OD_{LH}=\frac{1}{3k}$



$OD_{HL}=1/k$ $\quad OD_{LH}=\frac{1}{3}$

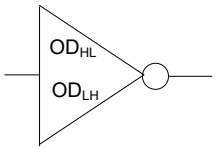
$FI=\frac{C_{REF}}{2}$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Minimum-sized gates

	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized
C_{IN}/C_{REF}			
Inverter	1	OD	1/2
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	1/2
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	1/2
Overdrive			
Inverter			
HL	1	OD	1
LH	1	OD	1/3
NOR			
HL	1	OD	1
LH	1	OD	1/(3k)
NAND			
HL	1	OD	1/k
LH	1	OD	1/3
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$

Minimum-sized gates



$F_{I2}=13/2$

$F_{I3}=1$

$F_{I4}=1$

$F_{I5}=1/2$

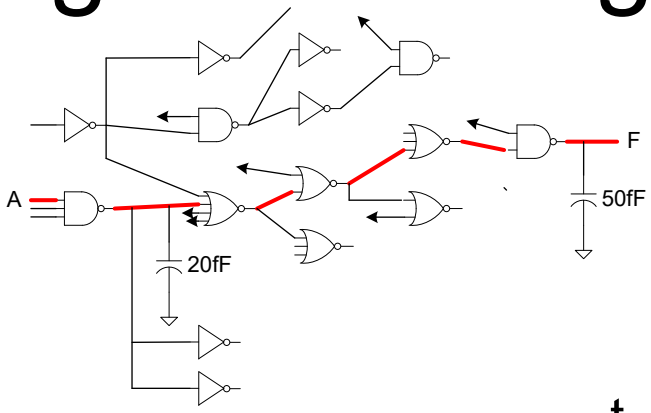
$F_{I6}=12.5$

$$t_{PROP}=t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

$$t_{PROP}=t_{REF} \bullet \frac{1}{2}\left(\frac{13}{2}(3+3)+1(12+1)+1(6+1)+\frac{1}{2}(9+1)+12.5(2+3) \right)$$

$$t_{PROP}=63.25 \bullet t_{REF}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading



- **Equal rise/fall (no overdrive)**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

- **Equal rise/fall with overdrive**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Minimum Sized**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Asymmetric Overdrive**

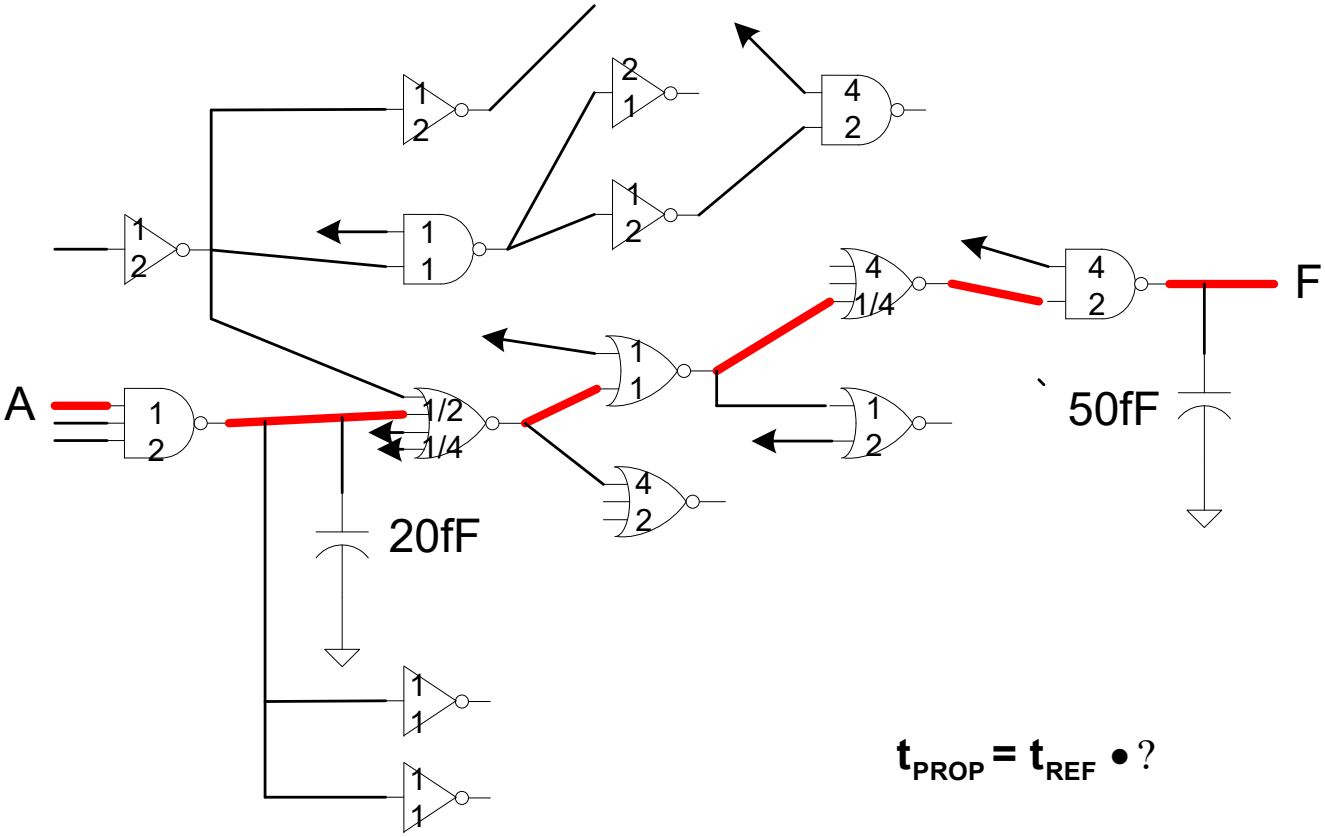
$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Combination of equal rise/fall, minimum size and overdrive**

$$t_{PROP} = \ ?$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates



$t_{PROP} = t_{REF} \bullet ?$

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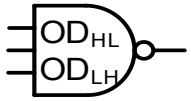
Asymmetric-sized gates

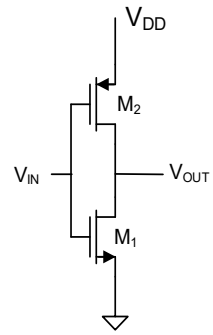


	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD_{HL}, OD_{LH})
C_{IN}/C_{REF}				
Inverter	1	OD	1/2	?
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	1/2	?
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	1/2	?
Overdrive				
Inverter				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/3	OD_{LH}
NOR				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/(3k)	OD_{LH}
NAND				
HL	1	OD	1/k	OD_{HL}
LH	1	OD	1/3	OD_{LH}
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$

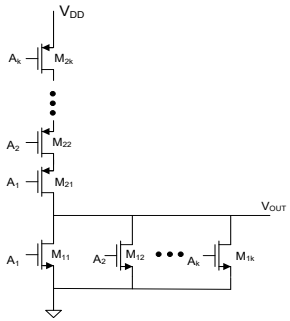
$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2}\sum_{k=1}^{5} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)\right)$$

Asymmetric-sized gates C_{IN}/C_{REF}

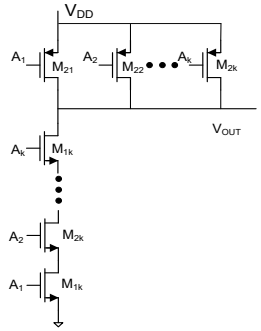
Inverter



NOR



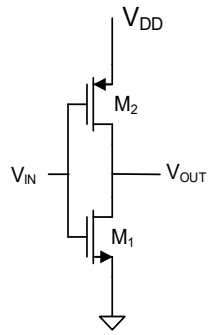
NAND



Asymmetric-sized gates C_{IN}/C_{REF}

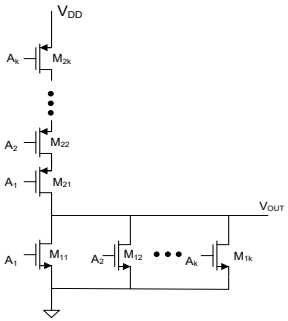
Inverter

$$\frac{C_{IN}}{C_{REF}} = \frac{C_{OX}W_n OD_{HL}L + C_{OX}(3W_n)OD_{LH}L}{4C_{OX}W_nL} = \frac{OD_{HL} + 3OD_{LH}}{4}$$



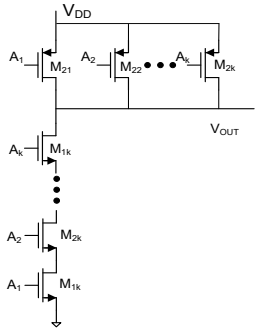
NOR

$$\frac{C_{IN}}{C_{REF}} = \frac{C_{OX}W_n OD_{HL}L + C_{OX}(3kW_n)OD_{LH}L}{4C_{OX}W_nL} = \frac{OD_{HL} + 3kOD_{LH}}{4}$$



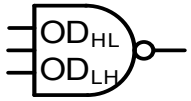
NAND

$$\frac{C_{IN}}{C_{REF}} = \frac{C_{OX}kW_n OD_{HL}L + C_{OX}(3W_n)OD_{LH}L}{4C_{OX}W_nL} = \frac{k \bullet OD_{HL} + 3OD_{LH}}{4}$$



Propagation Delay in Multiple-Levels of Logic with Stage Loading

Asymmetric-sized gates

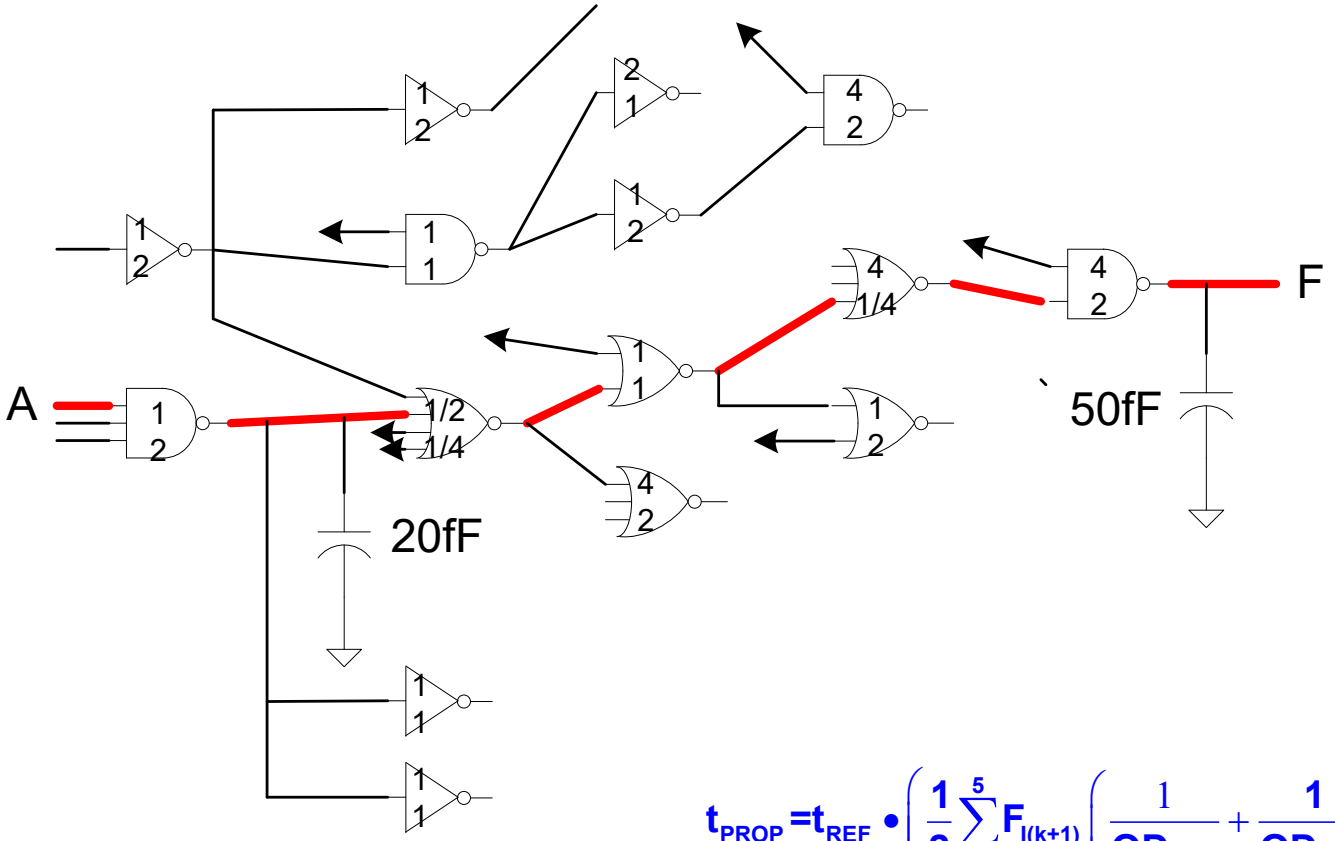


	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD_{HL}, OD_{LH})
C_{IN}/C_{REF}				
Inverter	1	OD	1/2	$\frac{OD_{HL}+3 \bullet OD_{LH}}{4}$
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	1/2	$\frac{OD_{HL}+3k \bullet OD_{LH}}{4}$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	1/2	$\frac{k \bullet OD_{HL}+3 \bullet OD_{LH}}{4}$
Overdrive				
Inverter				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/3	OD_{LH}
NOR				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/(3k)	OD_{LH}
NAND				
HL	1	OD	1/k	OD_{HL}
LH	1	OD	1/3	OD_{LH}
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2}\sum_{k=1}^{5} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)\right)$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

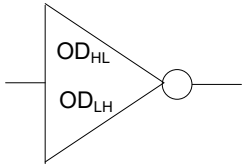
Asymmetric-sized gates



$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

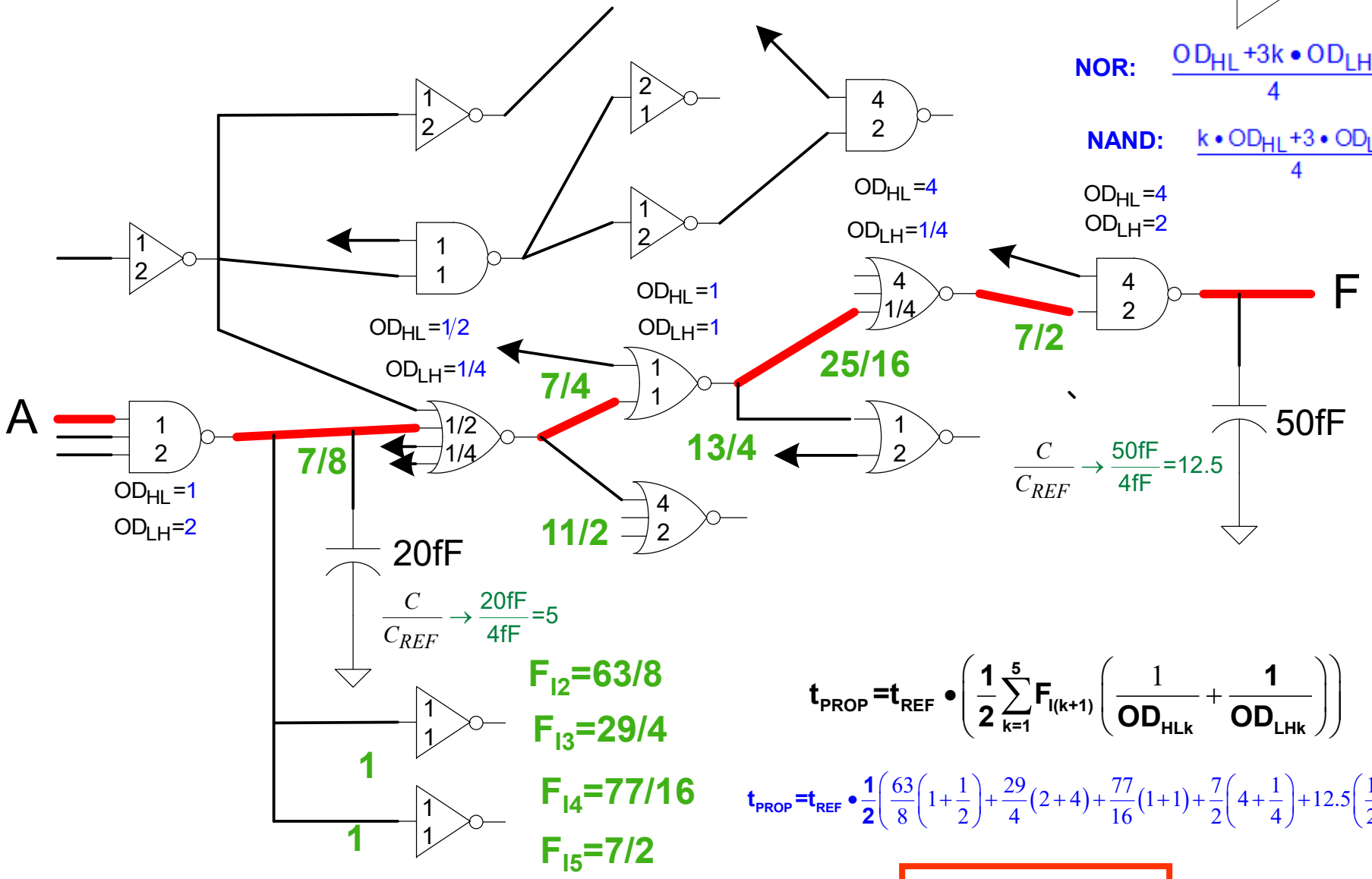
Asymmetric-sized gates

(Note: This C_{OX} is somewhat larger than that in the 0.5u ON process)



NOR: $\frac{OD_{HL}+3k \bullet OD_{LH}}{4}$

NAND: $\frac{k \bullet OD_{HL}+3 \bullet OD_{LH}}{4}$



$F_{I2}=63/8$

$F_{I3}=29/4$

$F_{I4}=77/16$

$F_{I5}=7/2$

$F_{I6}=12.5$

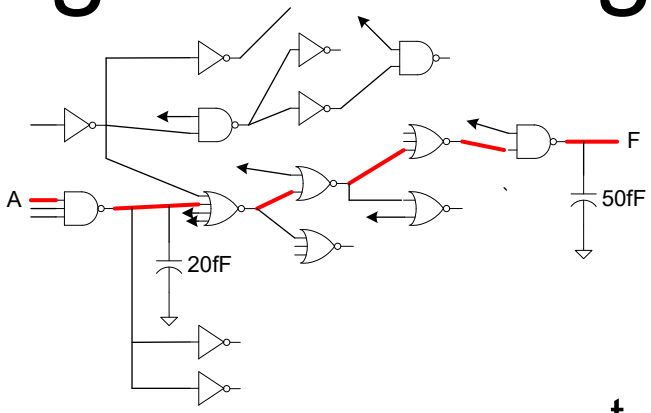
$$t_{PROP}=t_{REF} \bullet \left(\frac{1}{2}\sum_{k=1}^{5} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)\right)$$

$$t_{PROP}=t_{REF} \bullet \frac{1}{2}\left(\frac{63}{8}\left(1+\frac{1}{2}\right)+\frac{29}{4}(2+4)+\frac{77}{16}(1+1)+\frac{7}{2}\left(4+\frac{1}{4}\right)+12.5\left(\frac{1}{2}+\frac{1}{4}\right)\right)$$

$t_{PROP} = t_{REF} \bullet ?$

$$t_{PROP}=44.6 \bullet t_{REF}$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading



- **Equal rise/fall (no overdrive)**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} FI_{(k+1)}$$

- **Equal rise/fall with overdrive**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Minimum Sized**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Asymmetric Overdrive**

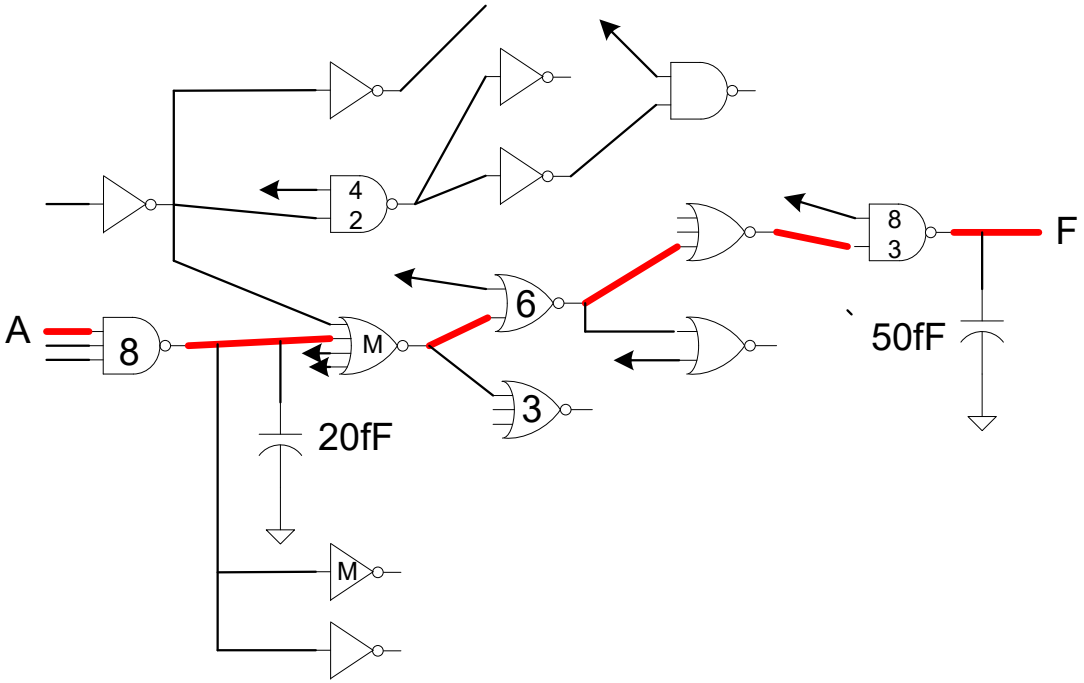
$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Combination of equal rise/fall, minimum size and overdrive**

$$t_{PROP} = \ ?$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading

Mixture of Minimum-sized gates, equal rise/fall gates and OD



$t_{PROP} = t_{REF} \bullet ?$

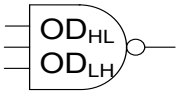
Driving Notation

- **Equal rise/fall (no overdrive)**

- **Equal rise/fall with overdrive**

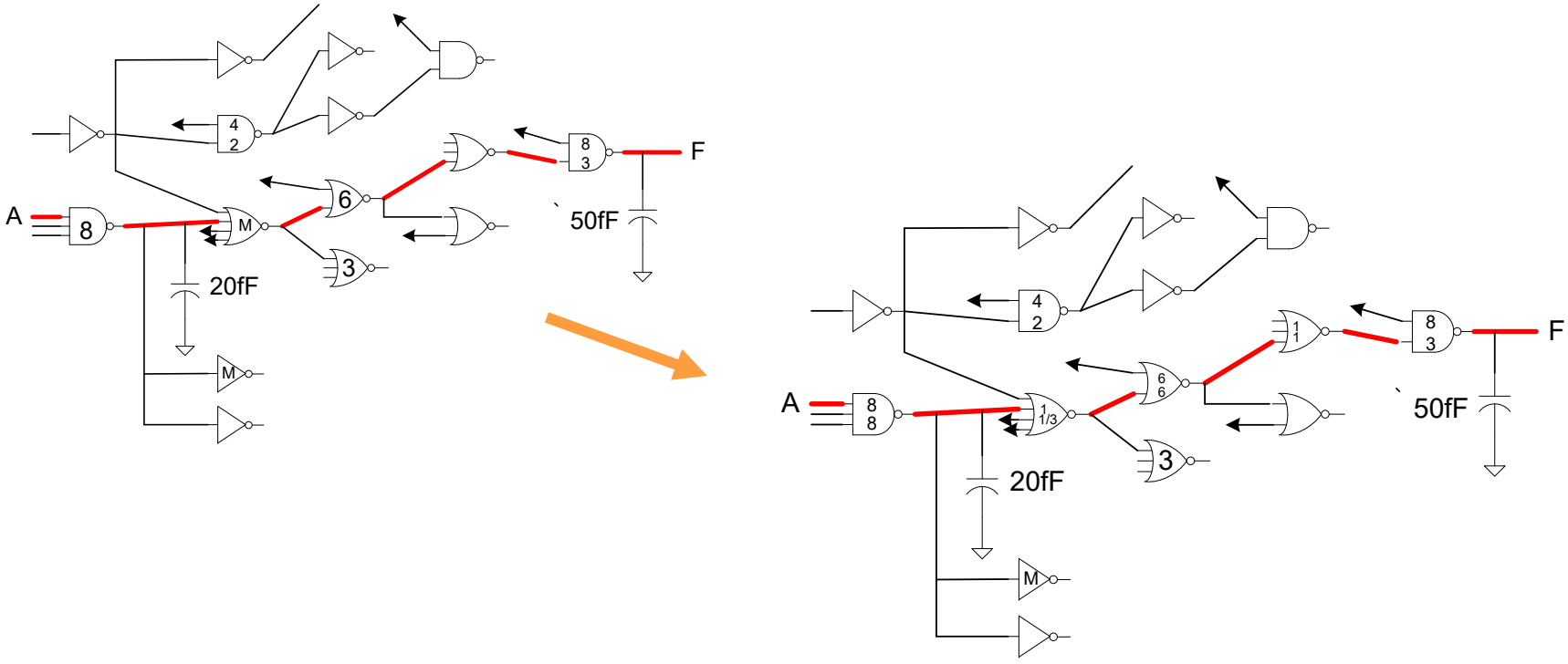
- **Minimum Sized**

- **Asymmetric Overdrive**



Propagation Delay in Multiple-Levels of Logic with Stage Loading

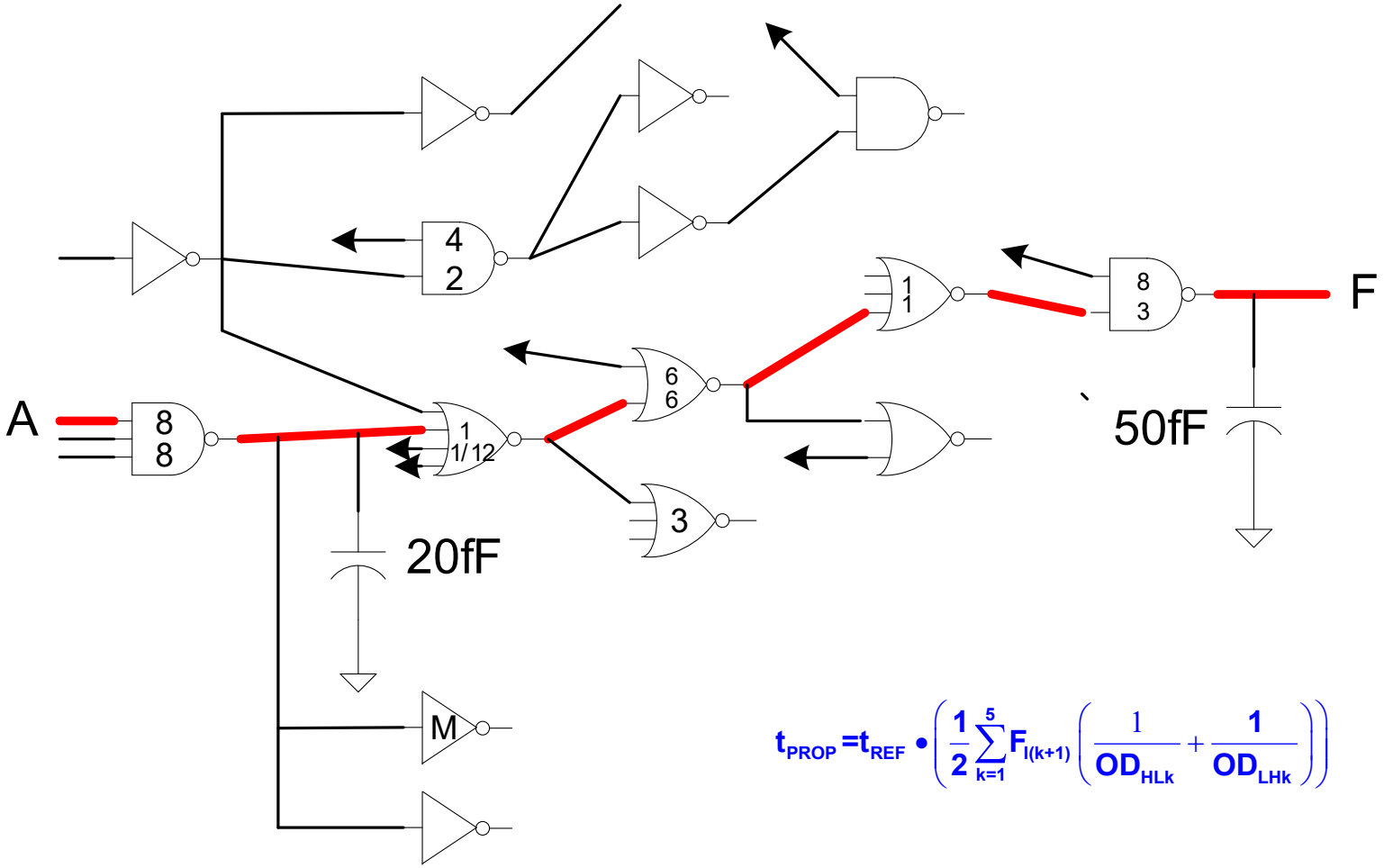
Mixture of Minimum-sized gates, equal rise/fall gates and OD



$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

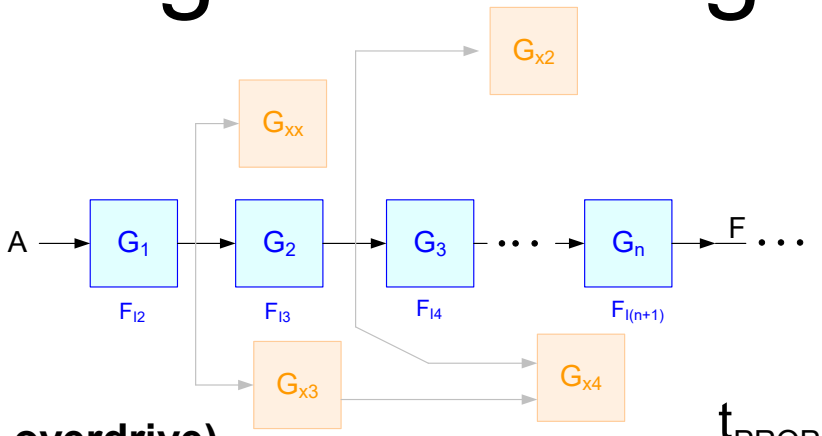
Propagation Delay in Multiple-Levels of Logic with Stage Loading

Mixture of Minimum-sized gates, equal rise/fall gates and OD



$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{5} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

Propagation Delay in Multiple-Levels of Logic with Stage Loading



- **Equal rise/fall (no overdrive)**

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- **Equal rise/fall with overdrive**

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Minimum Sized**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

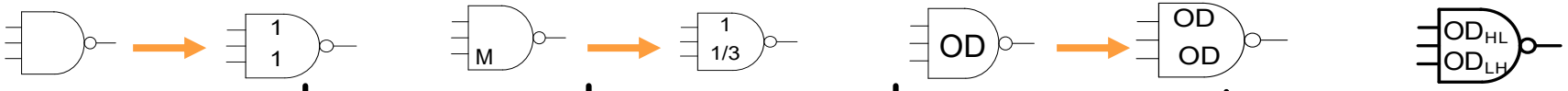
- **Asymmetric overdrive**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

- **Combination of equal rise/fall, minimum size and overdrive**

$$t_{PROP} = t_{REF} \bullet \left(\frac{1}{2} \sum_{k=1}^{n} F_{I(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right) \right)$$

Summary: Propagation Delay in Multiple-Levels of Logic with Stage Loading



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t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{I(k+1)}$	$\sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$	$\frac{1}{2}\sum_{k=1}^{n} F_{I(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$

Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
    - FI/OD
      - Logical Effort
  - Elmore Delay
- Sizing of Gates
  - The Reference Inverter

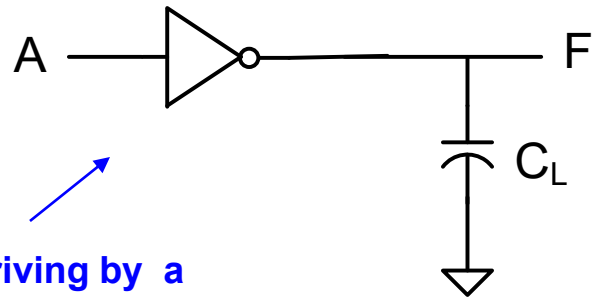
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators

done

partial

Driving Large Capacitive Loads

Example



Assume driving by a reference inverter

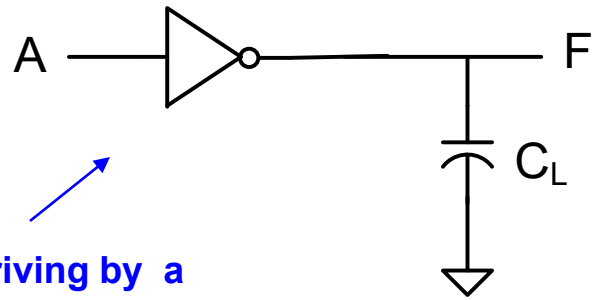
Assume $C_L=1000C_{REF}$

t_{PROP}=?

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

Driving Large Capacitive Loads

Example



Assume driving by a reference inverter

Assume $C_L=1000C_{REF}$

$t_{PROP}=1000t_{REF}$

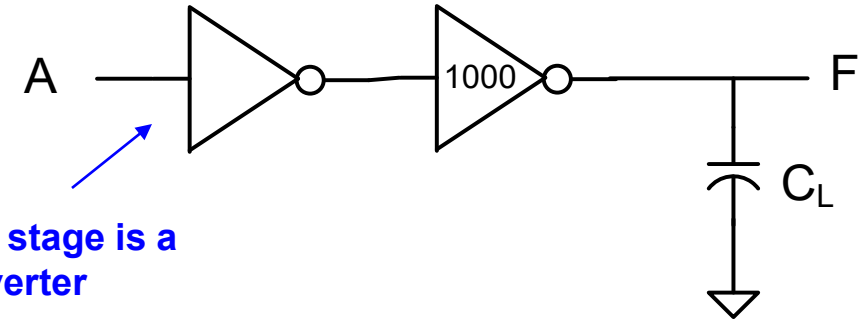
t_{PROP} is too long !

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

Driving Large Capacitive Loads

Example

Assume $C_L = 1000 C_{REF}$



Assume first stage is a reference inverter

$$t_{PROP} = ?$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{2} \frac{F_{I(k+1)}}{OD_k}$$

$$t_{PROP} = t_{REF} \left(\frac{1}{1} 1000 + \frac{1}{1000} 1000 \right) = t_{REF} \left(1000 + 1 \right)$$

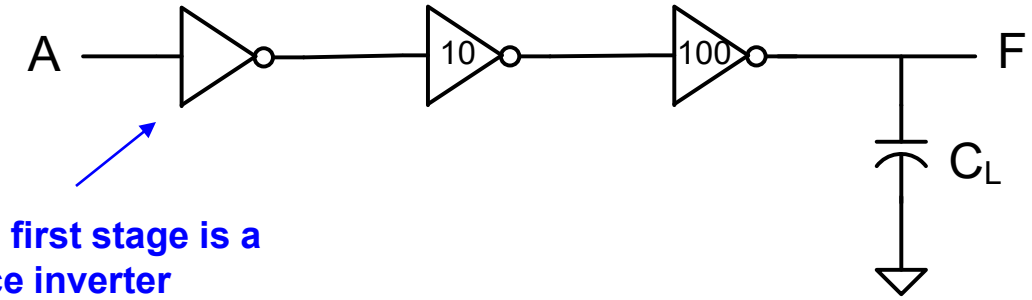
$$t_{PROP} = t_{REF} \left(1001 \right)$$

Delay of second inverter is really small but overall delay is even longer than before!

Driving Large Capacitive Loads

Example

Assume $C_L = 1000C_{REF}$



Assume first stage is a reference inverter

$$t_{PROP} = t_{REF} \sum_{k=1}^{3} \frac{F_{I(k+1)}}{OD_k}$$

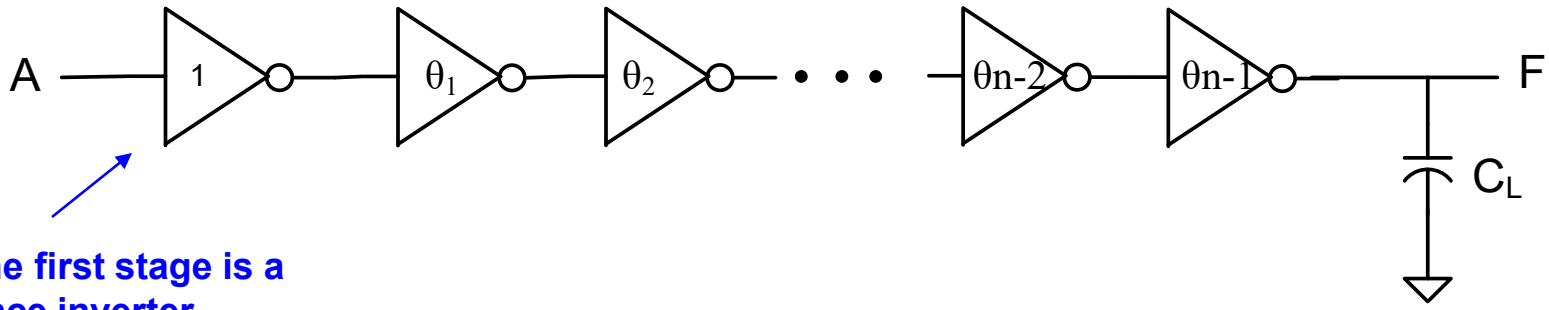
$$t_{PROP} = t_{REF} \left(\frac{1}{1}10 + \frac{1}{10}100 + \frac{1}{100}1000 \right) = t_{REF} \left(10 + 10 + 10 \right)$$

$$t_{PROP} = 30t_{REF}$$

Dramatic reduction is propagation delay (over a factor of 30!)

What is the fastest way to drive a large capacitive load?

Optimal Driving of Capacitive Loads



Assume first stage is a reference inverter

Need to determine the number of stages, n, and the OD factors for each stage to minimize t_{PROP}.

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k} \quad \rightarrow \quad t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}}$$

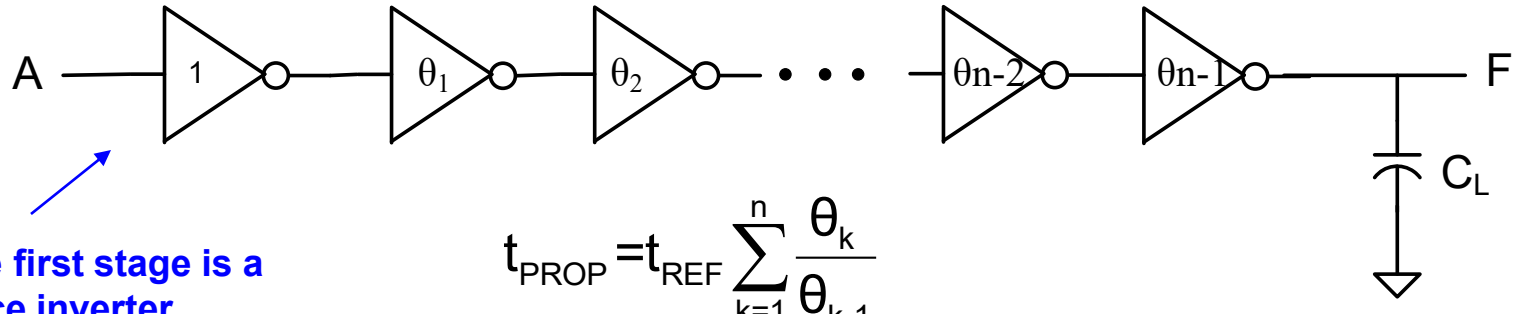
where $\theta_0 = 1$, $\theta_n = C_L / C_{REF}$

This becomes an n-parameter optimization (minimization) problem !

Unknown parameters: $\{\theta_1, \theta_2, \ldots \theta_{n-1}, n\}$

An n-parameter nonlinear optimization problem is generally difficult !!!!

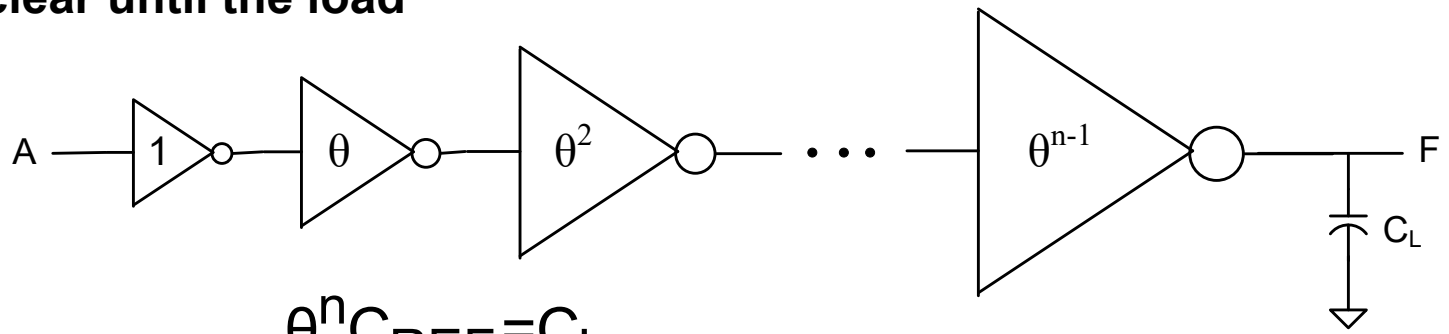
Optimal Driving of Capacitive Loads



Assume first stage is a reference inverter

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}}$$

Order reduction strategy : Assume overdrive of stages increases by the same factor clear until the load



$$\theta^n C_{REF} = C_L$$

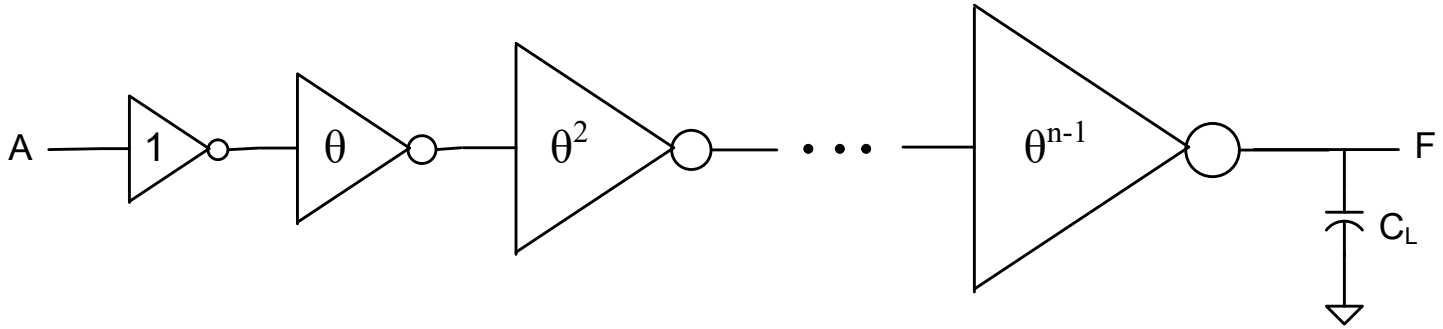
This becomes a 2-parameter optimization (minimization) problem !

Unknown parameters: $\{\theta, n\}$

One degree of freedom

One constraint : $\theta^n C_{REF} = C_L$

Optimal Driving of Capacitive Loads



$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{\theta_k}{\theta_{k-1}} \quad \rightarrow \quad t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{\theta^k}{\theta^{k-1}}$$

$$\theta^n C_{REF} = C_L \text{ or } FI_L = \theta^n$$

$$t_{PROP} = t_{REF} n\theta$$

$$\left.\begin{aligned} t_{PROP} &= t_{REF} n\theta \\ \theta^n C_{REF} &= C_L \end{aligned}\right\}$$

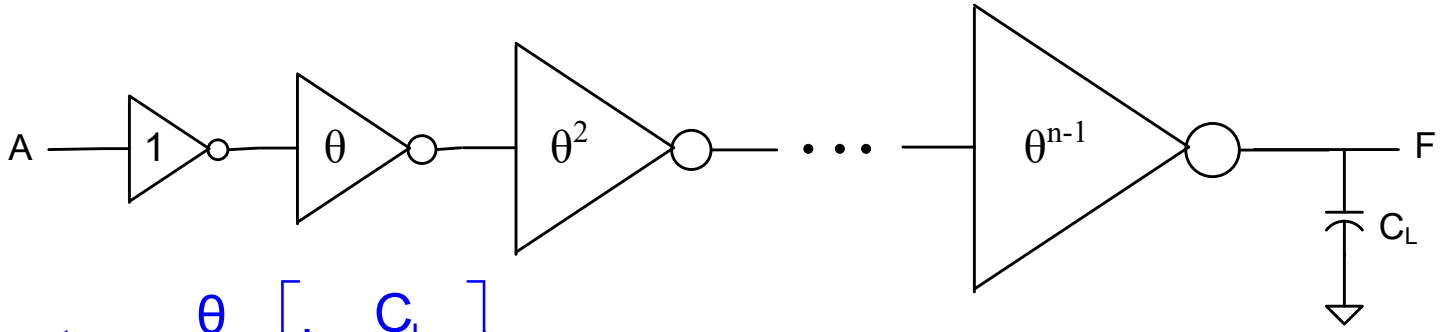
Unknown parameters: $\{\theta, n\}$

$$\theta^n C_{REF} = C_L \quad \rightarrow \quad n = \frac{1}{\ln(\theta)} \ln\left(\frac{C_L}{C_{REF}}\right)$$

Thus obtain an expression for t_{PROP} in terms of only θ

$$t_{PROP} = t_{REF} \frac{\theta}{\ln(\theta)} \left[\ln \frac{C_L}{C_{REF}}\right]$$

Optimal Driving of Capacitive Loads



$$t_{PROP} = t_{REF} \frac{\theta}{\ln(\theta)} \left[\ln \frac{C_L}{C_{REF}} \right]$$

$$\theta^n C_{REF} = C_L$$

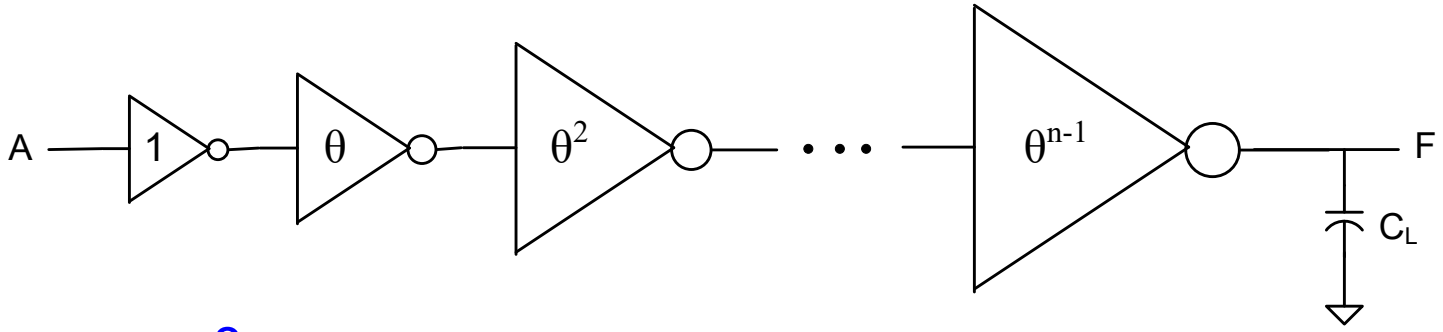
It suffices to minimize the function $f(\theta) = \frac{\theta}{\ln(\theta)}$

$$\frac{df}{d\theta} = \frac{\ln(\theta) - \theta \bullet \left(\frac{1}{\theta}\right)}{(\ln(\theta))^2} = 0$$

$$\ln(\theta) - 1 = 0 \quad \rightarrow \quad \theta = e$$

$$n = \frac{1}{\ln(\theta)} \ln\left(\frac{C_L}{C_{REF}}\right) \quad \rightarrow \quad n = \ln\left(\frac{C_L}{C_{REF}}\right) = \ln(F I_L)$$

Optimal Driving of Capacitive Loads



$$\theta_{OPT} = e$$

$$\theta^n C_{REF} = C_L$$

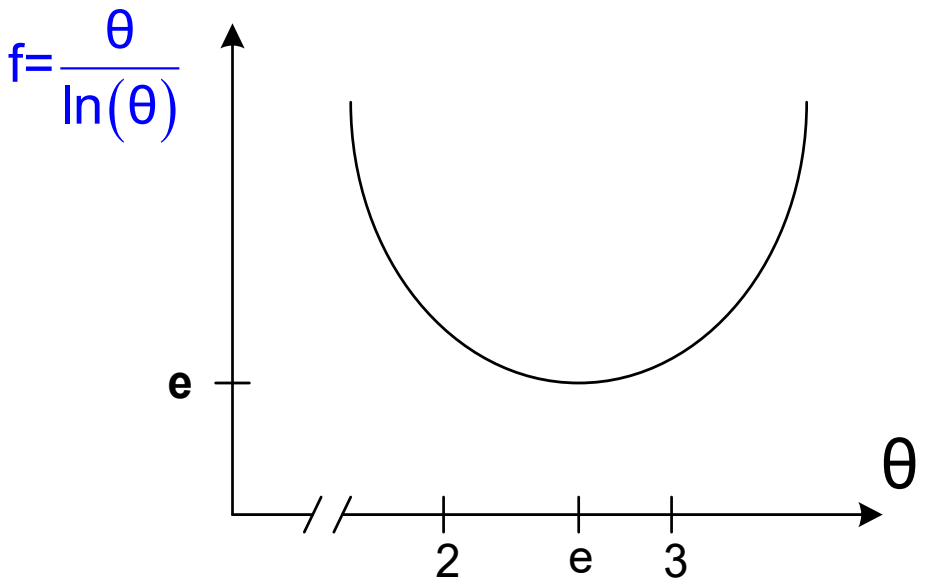
$$n_{OPT} = \ln\left(\frac{C_L}{C_{REF}}\right) = \ln(FI_L)$$

$$t_{PROP} = t_{REF}\frac{\theta}{\ln(\theta)}\left[\ln\frac{C_L}{C_{REF}}\right] \qquad t_{PROP} = t_{REF} e\left[\ln\frac{C_L}{C_{REF}}\right] = net_{REF}$$

- **Since $\theta_{OPT} = e$ is an irrational number, snap-size limitations in layout tools make it impossible to use the optimal scaling factor (even if n comes out to be an integer).**
- **Need a practical solution**

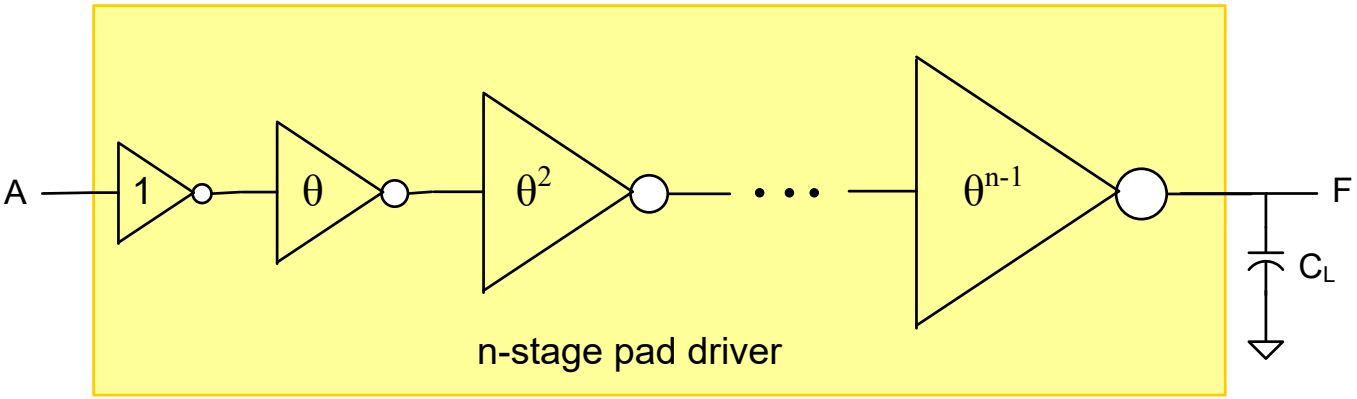
Optimal Driving of Capacitive Loads

A practical solution



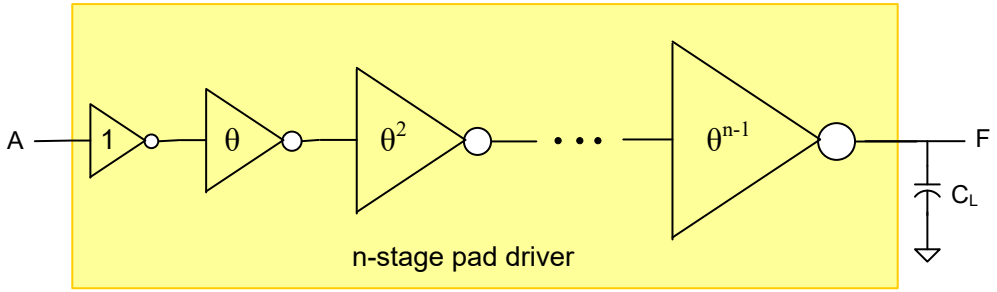
- **minimum at θ=e but shallow inflection point for 2<θ<3**
- **practically pick θ=2, θ=2.5, or θ=3**
- **since optimization may provide non-integer for n, must pick close integer**

Optimal Driving of Capacitive Loads



- **Often termed a pad driver**
- **Often used to drive large internal busses as well**
- **Generally included in standard cells or in cell library**
- **Device sizes can become very large**
- **Odd number of stages will cause signal inversion but usually not a problem**

Optimal Driving of Capacitive Loads



Example: Design a pad driver for driving a load capacitance of 10pF with equal rise/fall times, determine t_{PROP} for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

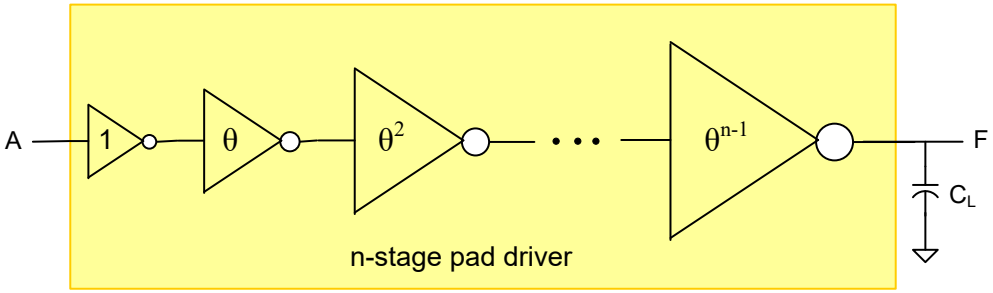
FI_L=2500

$$n_{OPT} = \ln\left(\frac{C_L}{C_{REF}}\right) = \ln\left(\frac{10pF}{4fF}\right) = \ln(2500) = 7.8$$

Select n=8, θ=2.5

$$W_{nk} = 2.5^{k-1} \bullet W_{REF}, \qquad W_{pk} = 3 \bullet 2.5^{k-1} \bullet W_{REF}$$

Optimal Driving of Capacitive Loads



Example: Design a pad driver for driving a load capacitance of 10pF with equal rise/fall times, determine t_{PROP} for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF,R_{PDREF}=2.5K

For θ = 2.5 , n=8 $W_{REF}=W_{MIN}$

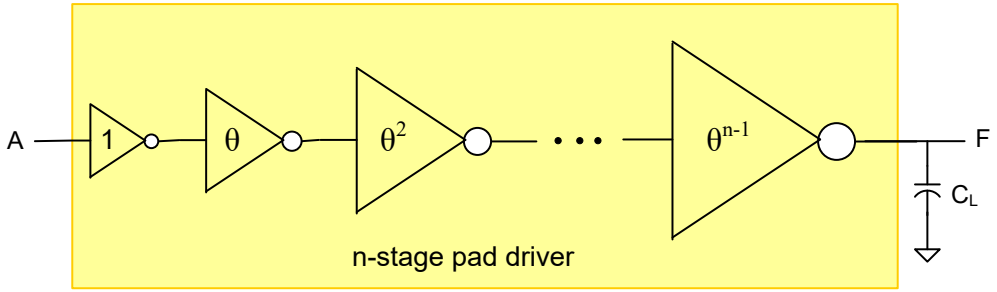
$W_{nk}=2.5^{k-1} \bullet W_{REF}$, $W_{pk}=3 \bullet 2.5^{k-1} \bullet W_{REF}$

$L_n=L_p=L_{MIN}$

k	n-channel		p-channel	
1	1	WMIN	3	WMIN
2	2.5	WMIN	7.5	WMIN
3	6.25	WMIN	18.75	WMIN
4	15.6	WMIN	46.9	WMIN
5	39.1	WMIN	117.2	WMIN
6	97.7	WMIN	293.0	WMIN
7	244.1	WMIN	732.4	WMIN
8	610.4	WMIN	1831.1	WMIN

Note devices in last stage are very large !

Optimal Driving of Capacitive Loads



Example: Design a pad driver for driving a load capacitance of 10pF with equal rise/fall times, determine t_{PROP} for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

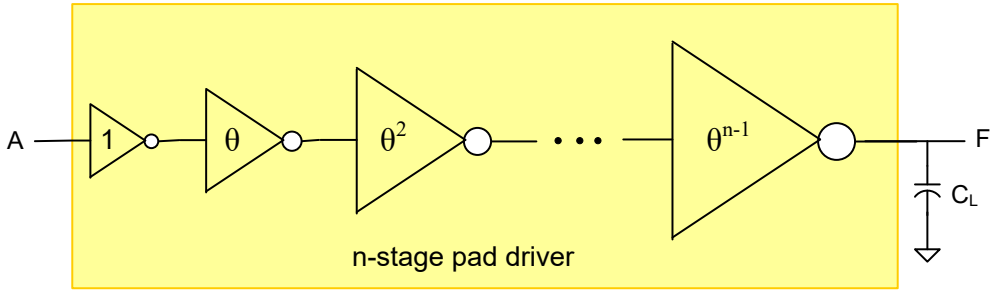
$W_{nk}=2.5^{k-1}\bullet W_{REF}$, $W_{pk}=3\bullet 2.5^{k-1}\bullet W_{REF}$

$$t_{PROP} \cong n\theta t_{REF} = 8\bullet 2.5\bullet t_{REF} = 20t_{REF}$$

More accurately:

$$t_{PROP}=t_{REF}\left(\sum_{k=1}^{7}\theta+\frac{1}{\theta^7}\frac{C_L}{C_{REF}}\right)=t_{REF}\left(17.5+\frac{1}{610}2500\right)=21.6t_{REF}$$

Optimal Driving of Capacitive Loads



More accurately:

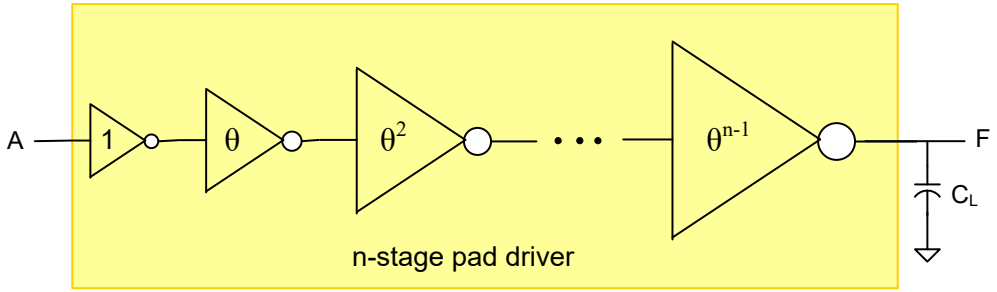
$$t_{PROP} = t_{REF}\left(\sum_{k=1}^{7}\theta + \frac{1}{\theta^7}\frac{C_L}{C_{REF}}\right) = t_{REF}\left(17.5 + \frac{1}{610}2500\right) = 21.6\,t_{REF}$$

Possible modest improvement for determining n and θ after determining n_{opt}:

Consider all possible combinations of θ in { 2 , 2.5 , 3} and
n in { INT(n_{opt}), 1+INT(n_{opt})}

$$t_{PROP}(\theta,n) = t_{REF}\left(\sum_{k=1}^{n-1}\theta + \frac{1}{\theta^{n-1}}\frac{C_L}{C_{REF}}\right) = t_{REF}\left((n-1)\theta + \frac{1}{\theta^{n-1}}FI_L\right)$$

Optimal Driving of Capacitive Loads



Example: Design a pad driver for driving a load capacitance of 10pF with equal rise/fall times, determine t_{PROP} for the pad driver, and compare this with the propagation delay for driving the pad with a minimum-sized reference inverter.

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

$$W_{nk}=2.5^{k-1}\bullet W_{REF},\qquad W_{pk}=3\bullet 2.5^{k-1}\bullet W_{REF}$$

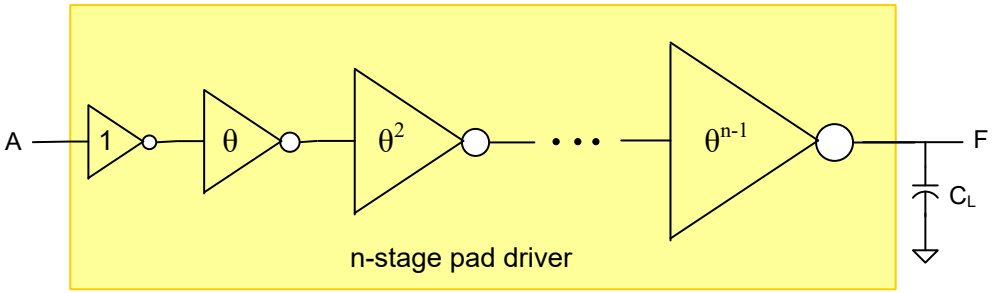
If driven directly with the minimum-sized reference inverter

$$t_{PROP}=t_{REF}\frac{C_L}{C_{REF}}=2500t_{REF}$$

Note an improvement in speed by a factor of approximately

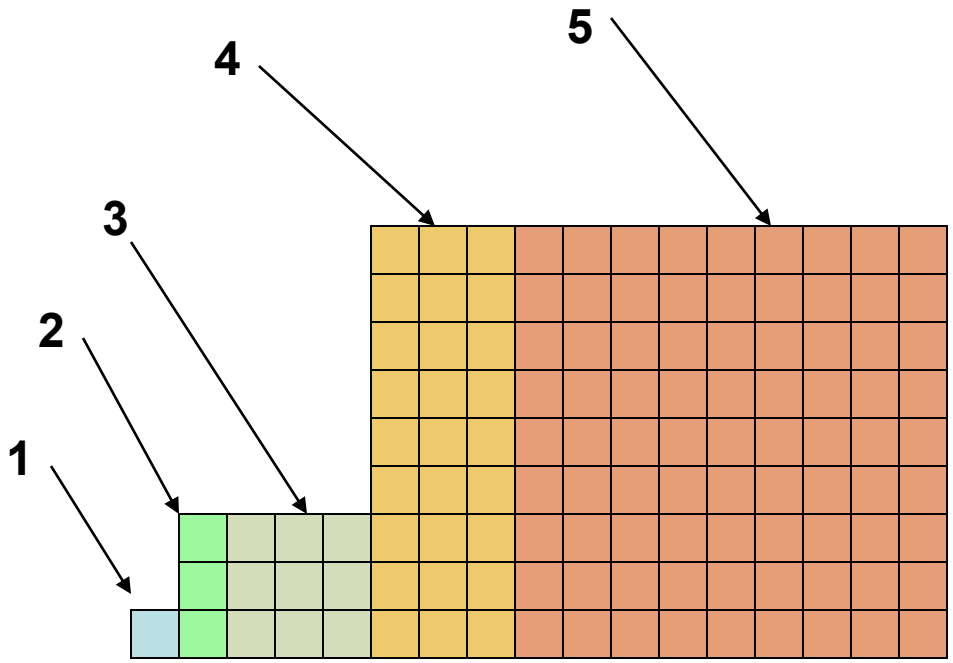
$$r=\frac{2500}{20}=125$$

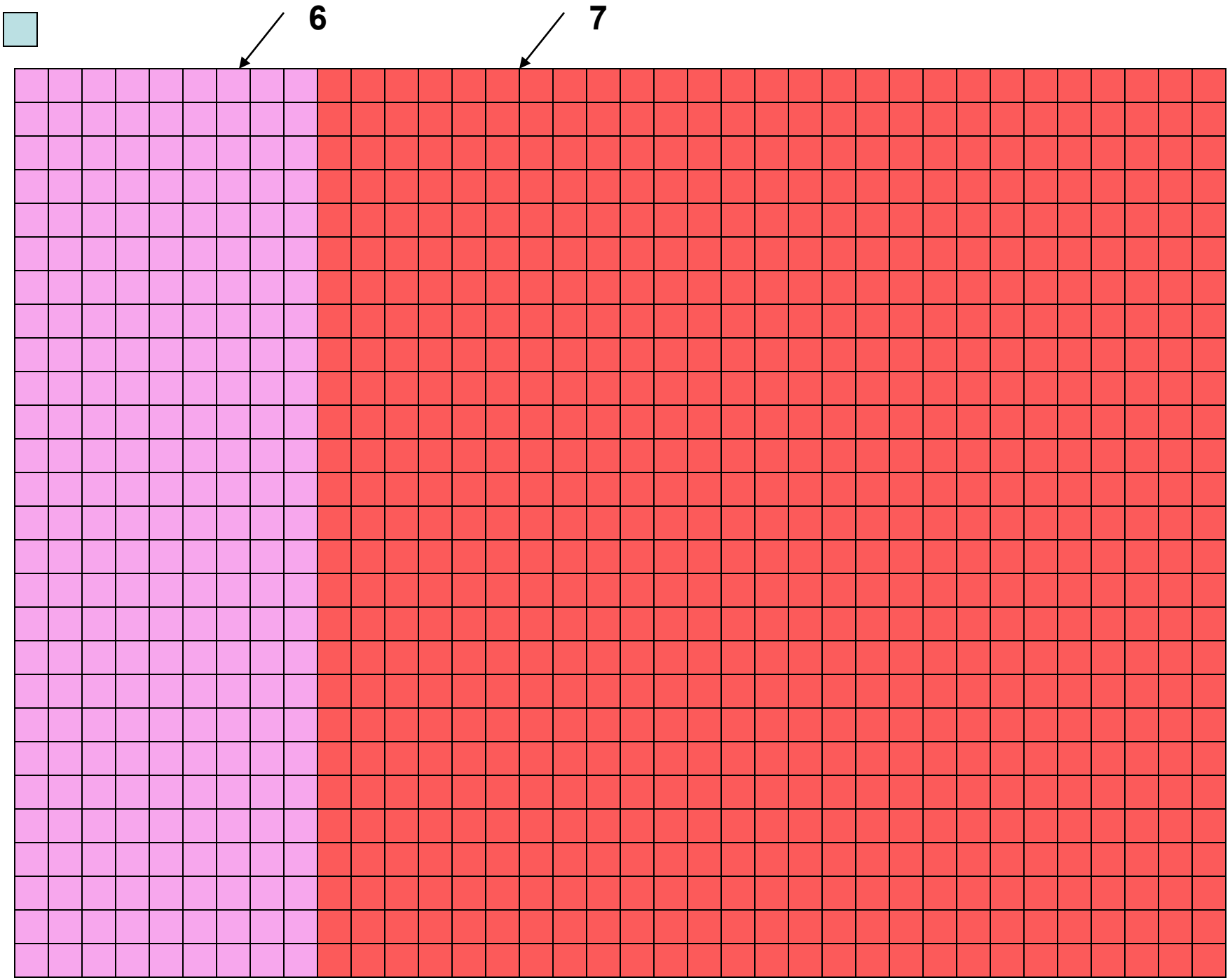
Pad Driver Size Implications



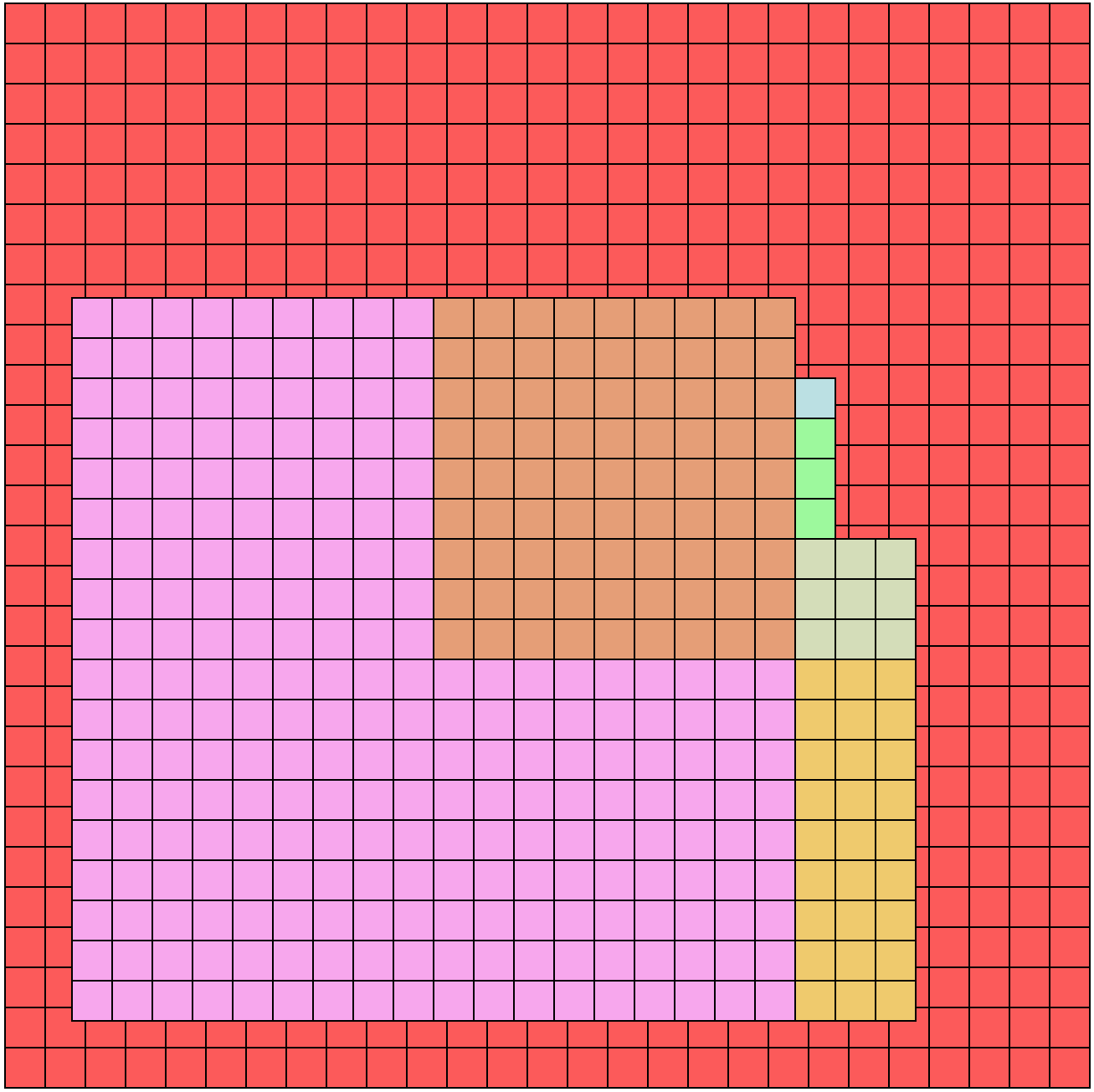
Consider a 7-stage pad driver and assume θ = 3

: Area of Ref Inverter




6
7

Area of Last Stage Larger than that of all previous stages combined!



Propagation Delay in “Logic Effort” approach

(Discussed in Chapter 4 of Text but definitions are not rigorous)

Logical effort

From Wikipedia, the free encyclopedia **(Dec 8, 2021)**

The method of **logical effort**, a term coined by Ivan Sutherland and Bob Sproull in 1991, is a straightforward technique used to estimate delay in a CMOS circuit. Used properly, it can aid in selection of gates for a given function (including the number of stages necessary) and sizing gates to achieve the minimum delay possible for a circuit.

Propagation Delay in "Logic Effort" approach

(Discussed in Chapter 4 of Text but definitions are not rigorous)

Propagation delay for equal rise/fall gates was derived to be

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

Delay calculations with "logical effort" approach

Logical effort delay approach:

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k$$

(t_{REF} scaling factor not explicitly stated in W_H textbook. As defined in W_H, f_k is dimensionless)

where f_k is the "effort delay" of stage k

$$f_k = g_k h_k$$

g_k=logical effort

h_k=electrical effort

Propagation Delay in “Logic Effort” approach

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k \qquad f_k = g_k h_k$$

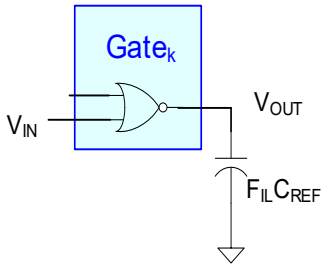
f_k = “effort delay” of stage k

g_k=logical effort

h_k=electrical effort

Logic Effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current

Electrical Effort is the ratio of the gate load capacitance to the input capacitance of a gate

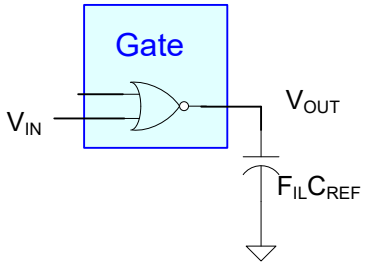


Propagation Delay in “Logic Effort” approach

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k \qquad f_k = g_k h_k$$

Logic Effort (g) is the ratio of the input capacitance of a gate to the input capacitance of an inverter that can deliver the same output current

Electrical Effort (h) is the ratio of the gate load capacitance to the input capacitance of a gate



$$g_k = \frac{C_{IN_k}}{C_{REF} \bullet OD_k} \qquad h_k = \frac{C_{REF} \bullet FI_{k+1}}{C_{IN_k}}$$

Propagation Delay in “Logic Effort” approach

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k \qquad f_k = g_k h_k$$

$$g_k = \frac{C_{IN_k}}{C_{REF} \bullet OD_k} \qquad h_k = \frac{C_{REF} \bullet F_{I(k+1)}}{C_{IN_k}}$$

$$f_k = \left(\frac{C_{IN_k}}{C_{REF} \bullet OD_k} \right) \left(\frac{C_{REF} \bullet F_{I(k+1)}}{C_{IN_k}} \right)$$

$$f_k = \frac{F_{I(k+1)}}{OD_k}$$

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k = t_{REF} \sum_{k=1}^{n} g_k h_k = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

Propagation Delay in “Logic Effort” approach

$$t_{PROP} = t_{REF} \sum_{k=1}^{n} f_k = t_{REF} \sum_{k=1}^{n} g_k h_k = t_{REF} \sum_{k=1}^{n} \frac{F_{I(k+1)}}{OD_k}$$

- **Note this expression is identical to what we have derived previously**
  (t_{REF} scaling factor not included in W_H text)

- **Probably more tedious to use the “Logical Effort” approach**
- **Extensions to asymmetric overdrive factors may not be trivial**
- **Extensions to include parasitics may be tedious as well**
- **Logical Effort is widely used throughout the industry**

Stay Safe and Stay Healthy !

End of Lecture 42